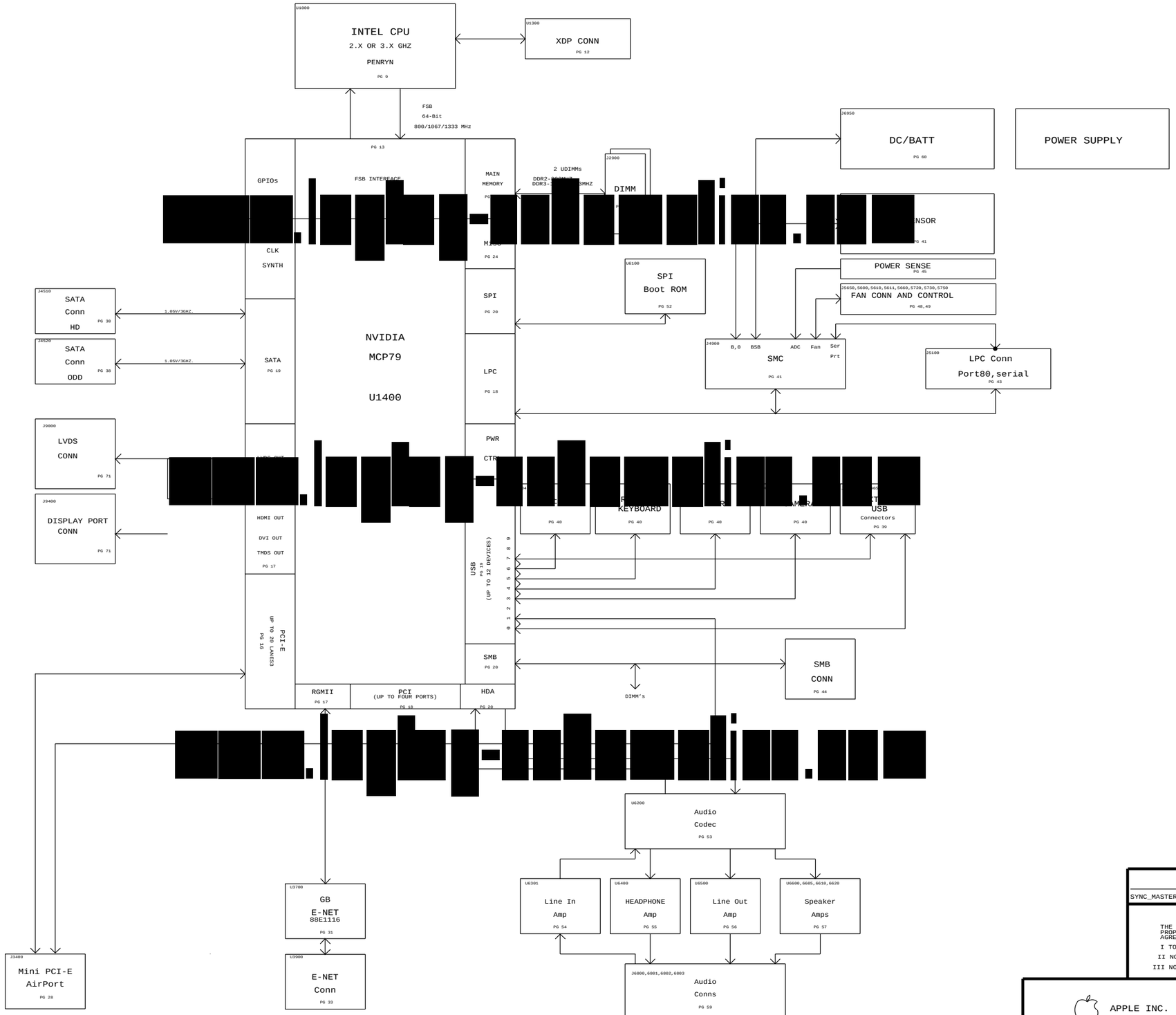
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEMATIC,Folsten_MBP17

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
B		738810	Production Release	6/19/09	6/19/09

06/15/09

Page (.csa)		Contents	Sync	Date
1	1	Table of Contents	K20_MLB	04/01/2008
2	2	System Block Diagram	M98_MLB	04/01/2008
3	3	Power Block Diagram	RXU_K20	07/24/2008
4	4	Revision History	NA	NA
5	5	BOM Configuration	[redacted]	[redacted]
6	6	JTAG Scan Chain	[redacted]	[redacted]
7	7	Functional / ICT Test	[redacted]	[redacted]
8	8	Power Aliases	RXU_K20	[redacted]
9	9	Signal Aliases	K20_MLB	09/24/2008
10	10	CPU FSB	M98_MLB	04/01/2008
11	11	CPU Power & Ground	M98_MLB	04/01/2008
12	12	CPU Decoupling & VID	M98_MLB	04/01/2008
13	13	eXtended Debug Port(MiniXDP)	M98_MLB	04/01/2008
14	14	MCP CPU Interface	T18_MLB	06/06/2008
15	15	MCP Memory Interface	T18_MLB	06/06/2008
16	16	MCP Memory Misc	T18_MLB	06/06/2008
17	17	MCP PCIe Interfaces	T18_MLB	06/06/2008
18	18	MCP Ethernet & Graphics	T18_MLB	06/06/2008
19	19	MCP PCI & LPC	T18_MLB	06/06/2008
20	20	MCP SATA & USB	T18_MLB	06/06/2008
21	21	MCP HDA & MISC	T18_MLB	06/06/2008
22	22	MCP Power & Ground	[redacted]	06/06/2008
23	25	MCP Standard Decoupling	[redacted]	[redacted]
24	26	MCP Graphics Support	[redacted]	[redacted]
25	28	SB Misc	[redacted]	[redacted]
26	29	FSB/DDR3/FRAMEBUF Vref Margining	BEN_K20	10/15/2008
27	31	DDR3 SO-DIMM Connector A	BEN_K20	06/10/2008
28	32	DDR3 SO-DIMM Connector B	BEN_K20	07/14/2008
29	33	DDR3 Support	M98_MLB	04/01/2008
30	34	Right Clutch Connector	M98_MLB	05/01/2008
31	35	ExpressCard Connector	BEN_K20	10/15/2008
32	37	Ethernet PHY (RTL8211CL)	SUMA_K20	07/22/2008
33	38	Ethernet & AirPort Support	SUMA_K20	07/15/2008
34	39	Ethernet Connector	SUMA_K20	07/15/2008
35	41	FireWire LLC/PHY (FW643)	M98_MLB	04/01/2008
36	42	FireWire Port Power	YWU_K20	05/28/2008
37	43	FireWire Ports	M98_MLB	07/14/2008
38	45	SATA Connectors	M98_MLB	05/01/2008
39	46	External USB Connectors	M98_MLB	07/14/2008
40	48	Front Flex Support	[redacted]	07/18/2008
41	49	SMC	[redacted]	[redacted]
42	50	SMC Support	[redacted]	[redacted]
43	51	LPC+SPI Debug Connector	[redacted]	[redacted]
44	52	K20 SMBUS CONNECTIONS	BEN_K20	07/22/2008
45	53	Current & Voltage Sensing	YWU_K20	08/20/2008
46	54	Current Sensing	YWU_K20	08/12/2008
47	55	Thermal Sensors	YWU_K20	05/28/2008
48	56	Fan Connectors	M98_MLB	04/01/2008
4[redacted]	57	WELLSPRING 1	YMA_K20	05/19/2008
[redacted]	[redacted]	[redacted]	[redacted]	[redacted]



System Block Diagram

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

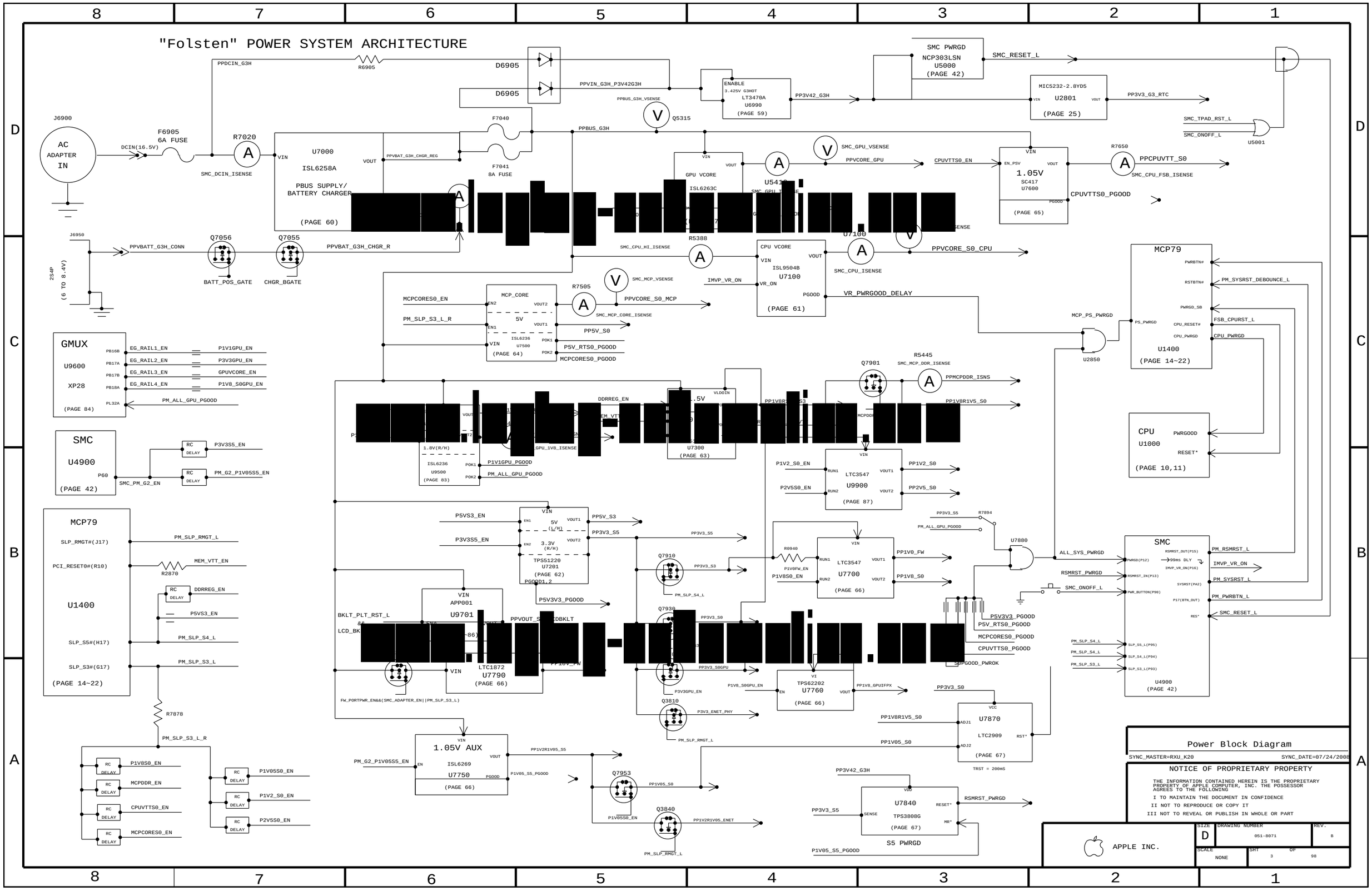
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 2 OF 98	

"Folsten" POWER SYSTEM ARCHITECTURE



Power Block Diagram

SYNC_MASTER=RXU_K20 SYNC_DATE=07/24/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 3 OF 98	

PVT:

03/24/09
csa.5: Project copied from K20 mlb_pvt.
Changed CPU APNs for 2.8 and 3.06GHz CPUs.
Changed BOM and EEE codes for K20A.
csa.45: Connected =PP1V5_EXP_S0 to J4501.13 for SATA redriver on flex.
03/25/09
csa.9: Added PBUS VS 5V voltage selection resistors for keyboard backlight driver.
03/27/09
csa.90: Added 1000pF cap to the backlight power pin for EMI baseline noise.
03/30/09
csa.5: Changed the bom option to KBDLED_5V per radar# 6723272.
03/31/09
csa.1: Changed rev to 1.0.0
04/09/09
csa.70: No stuff C7099 per radar# 6772695.
04/29/09
Production Release Fab to rev A
csa.5: Changed K20A EFI ROM APN 341S2507 (BOM change only)
05/05/09
Added 128S0264 (SANYO) as alternate to 128S0257 (KEMET ELEC) per Radar# 6656624.
06/15/09
Added 107S0136 (DALE/VISHAY) as alternate to 107S0132 (CYNTEC) per Radar# 6971400.
For U7871 P/N 353S2718 is made primary. P/N 353S2310 is added back as alternate.
For U6100 Locked Bootrom P/N 341S2506 replaces existing Unlock Bootrom P/N 341S2507.

www.laptop-motherboard.com

www.laptop-motherboard.com

www.laptop-motherboard.com

Revision History

SYNC_MASTER=NA SYNC_DATE=NA

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 4 OF 98

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0172	PCBA,BEST,2.8,512SAM_VRAM,K20A	K20A_COMMON,EEE_9EH,CPU_2_80GHZ,FB_512_SAMSUNG
639-0173	PCBA,BEST,3.06,512SAM_VRAM,K20A	K20A_COMMON,EEE_9EK,CPU_3_06GHZ,FB_512_SAMSUNG
639-0174	PCBA,BEST,2.8,512HYN_VRAM,K20A	K20A_COMMON,EEE_9EL,CPU_2_80GHZ,FB_512_HYNIX
639-0175	PCBA,BEST,3.06,512HYN_VRAM,K20A	K20A_COMMON,EEE_9EM,CPU_3_06GHZ,FB_512_HYNIX

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0476	152S0276		ALL	Inductor alternate
353S1681	353S1294		ALL	TI alt to National
138S0603	138S0602		ALL	Murata alt to Samsung
152S0684	152S0368		ALL	Maglayers alt to Dale/Vishay
104S0023	104S0018		ALL	Cyntec alt to sense resistor
104S0024	104S0017		ALL	Panasonic alt to FW resistor
341S2367	341S2366		ALL	Macronix alt to SST
152S0876	152S0782		ALL	Maglayer alt to Delta
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
514-0612	514-0607		ALL	FOXLINK ALT TO FOXCONN XCVR
514-0613	[redacted]		ALL	[redacted] ALT TO FOXCONN RCVR
[redacted]	[redacted]		[redacted]	[redacted]
[redacted]	[redacted]		[redacted]	[redacted]
[redacted]	[redacted]		[redacted]	[redacted]
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
128S0264	128S0257		ALL	SANYO ALT TO KEMET ELEC.
107S0136	107S0132		ALL	DALE/VISHAY ALT TO CYNTEC.
353S2310	353S2718		ALL	INTERSIL.COMMON TO K24/K19

Folsten BOM GROUPS

BOM GROUP	BOM OPTIONS
K20A_COMMON	ALTERNATE,COMMON,K20A_COMMON1,K20A[redacted]GPA[redacted]
K20A_COMMON1	ONEWIRE_PU,ISL6258,MEMRESET_HW,MEMRESET_MCP,MCP_B03,MCP_PROD,MCPSEQ_S[redacted]PROD[redacted]
K20A_COMMON2	BOOT_MODE_USER,GPUVID_1P00V,MUXGFX,DPMUX_EN_S0,DP_ESD,[redacted]
K20A_DEBUG	SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN
K20A_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_1024_SAMSUNG	VRAM8,VRAM_1024_SAMSUNG
FB_512_SAMSUNG	VRAM4,VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM4,VRAM_512_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRI[redacted]	[redacted]
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9EH]	CR[redacted]	[redacted]
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9EK]	CRITICAL	EEE_9EK
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9EL]	CRITICAL	EEE_9EL
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9EM]	CRITICAL	EEE_9EM

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0737	1	IC,ASSP,GPU,NV G96-GS,VLOWLKG,BGA969,LF	U8000	CRITICAL	
338S0694	1	IC,RTL8251CA-VB-GR,GIGE TRANSCEIVER,48P LQFP	U3700	CRITICAL	
338S0654	1	IC,FW643-E,1394B PHY/DHCI LINK/PCI-E,12	U4100	CRITICAL	
338S0710	1	IC,MCP79XT-B3,35X35MM,BGA1437	U1400	CRITICAL	MCP_B03
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2355	1	IC,SMC,DEVELOPMENT,K20	U4900	[redacted]	[redacted]
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	[redacted]	[redacted]
341S2506	1	IC,LOCKED EFI ROM,K20A	U6100	[redacted]	[redacted]
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
341S2383	1	IC,PSOC +W/USB,56PIN,MLF,M98	U5701	CRITICAL	TPAD_PROG
337S3744	1	IC,PDC,SLGKH,PMQ,3.06,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_3_06GHZ
337S3682	1	IC,PDC,SLGEM,PMQ,2.80,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_80GHZ
333S0481	4	IC,SGRAM,GDDR3,32MX32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0481	8	IC,SGRAM,GDDR3,32MX32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550,U9100,U9150,U9300,U9250	CRITICAL	VRAM_1024_SAMSUNG
333S0506	4	IC,SDRAM,GDDR3,32MX32,900MHZ,TIVA,HF	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_HYNIX

BOM Configuration

SYNC_MASTER=K20A_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

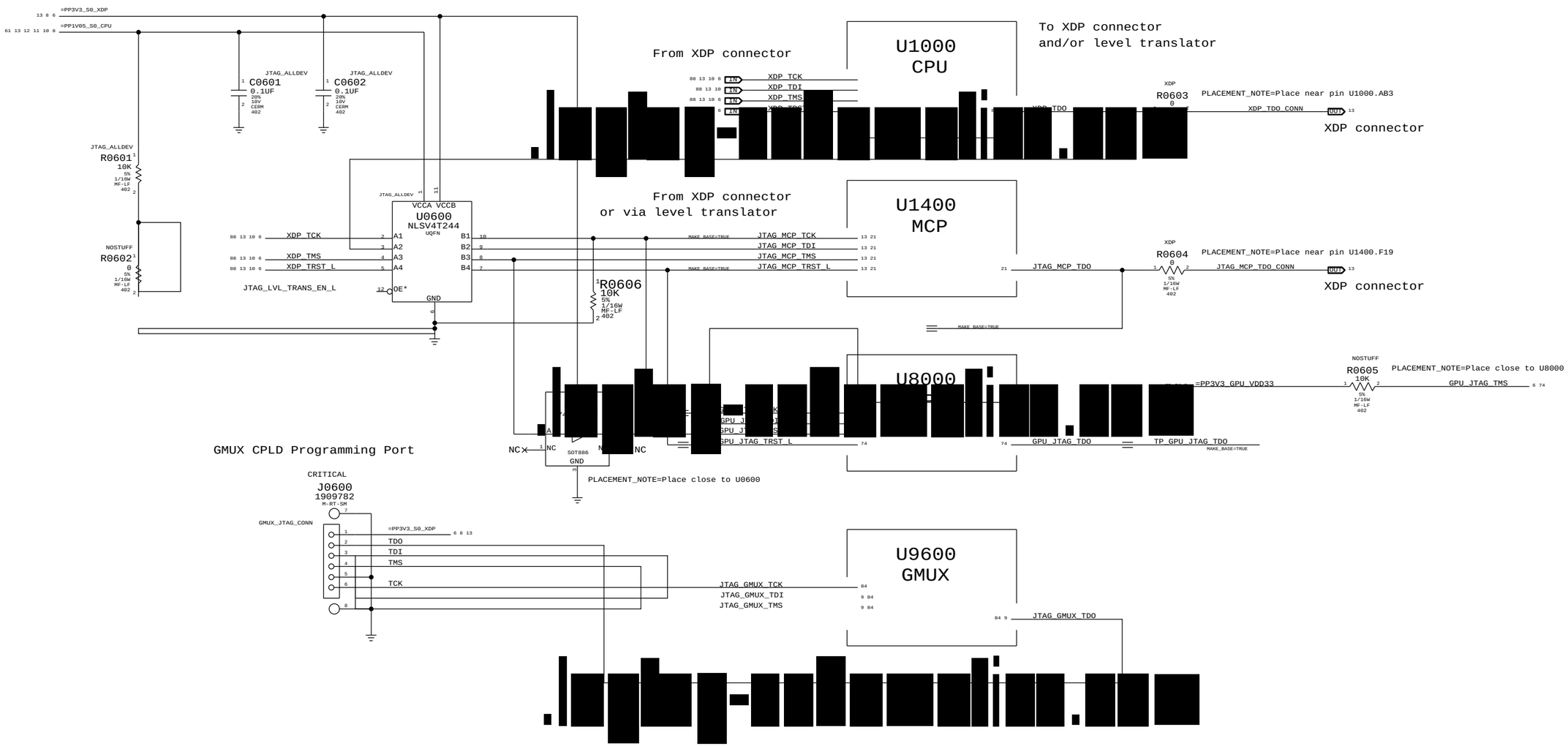
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 5 OF 98	

1.05V TO 3.3V LEVEL TRANSLATOR (M98: ON ICT FIXTURE)



JTAG Scan Chain

SYNC_MASTER=BEN_K20 SYNC_DATE=07/11/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 6 OF 98	

Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST

TRUE	=PP5V_S0_FAN_LT	8 48	3 TPs per Fan
TRUE	FAN_LT_PWM	48	
TRUE	FAN_LT_TACH	48	

J5660 (RIGHT FAN CONN)

TRUE	FAN_RT_PWM	48	
TRUE	FAN_RT_TACH	48	
TRUE	GND		5 TPs per Fan

J6780 (MIC CONN)

TRUE	BI_MIC_LO	57 58	
TRUE	BI_MIC_SHIELD	57 58	
TRUE	BI_MIC_HI	57 58	

J6781 (LEFT SPEAKER)

TRUE	SPKRAMP_L1_OUT_P	56 57 96
TRUE	SPKRAMP_L1_OUT_N	56 57 96
TRUE	SPKRAMP_L2_OUT_P	56 57 96
TRUE	SPKRAMP_L2_OUT_N	56 57 96

J6782 (RIGHT & SUB SPEAKER)

TRUE	SPKRAMP_LFE_OUT_P	56 57 96
TRUE	SPKRAMP_LFE_OUT_N	56 57 96
TRUE	SPKRAMP_R1_OUT_P	56 57 96
TRUE	SPKRAMP_R1_OUT_N	56 57 96
TRUE	SPKRAMP_R2_OUT_P	56 57 96
TRUE	SPKRAMP_R2_OUT_N	56 57 96

J9000 (LVDS CONN)

TRUE	BKL_SYNC	78 85	
TRUE	PP3V3_SW_LCD	78	
TRUE	=PP3V3_S0_DDC_LCD	8 75 78	
TRUE	PPVOUT_S0_LCDBKLT	78 85	2 TP needed
TRUE	LVDS_DDC_CLK	78 81	
TRUE	LVDS_DDC_DATA	78 81	
TRUE	LVDS_CONN_A_DATA_P<0>	78 81 95	
TRUE	LVDS_CONN_A_DATA_N<0>	78 81 95	
TRUE	LVDS_CONN_A_DATA_P<1>	78 81 95	
TRUE	LVDS_CONN_A_DATA_N<1>	78 81 95	
TRUE	LVDS_CONN_A_DATA_P<2>	78 81 95	
TRUE	LVDS_CONN_A_DATA_N<2>	78 81 95	
TRUE	LVDS_CONN_A_CLK_F_P	78 95	
TRUE	LVDS_CONN_A_CLK_F_N	78 95	
TRUE	LVDS_CONN_B_DATA_P<0>	78 81 95	
TRUE	LVDS_CONN_B_DATA_N<0>	78 81 95	
TRUE	LVDS_CONN_B_DATA_P<1>	78 81 95	
TRUE	LVDS_CONN_B_DATA_N<1>	78 81 95	
TRUE	LVDS_CONN_B_DATA_P<2>	78 81 95	
TRUE	LVDS_CONN_B_DATA_N<2>	78 81 95	
TRUE	LVDS_CONN_B_CLK_F_P	78 95	
TRUE	LVDS_CONN_B_CLK_F_N	78 95	
TRUE	LED_RETURN_1	78 85	
TRUE	LED_RETURN_2	78 85	
TRUE	LED_RETURN_3	78 85	
TRUE	LED_RETURN_4	78 85	
TRUE	LED_RETURN_5	78 85	
TRUE	LED_RETURN_6	78 85	
TRUE	GND		4 TPs

J4500 (SATA ODD CONN)

TRUE	PP5V_SW_ODD	38	
TRUE	SMC_ODD_DETECT	38 41	3 TPs
TRUE	SATA_ODD_D2R_C_P	38 90	
TRUE	SATA_ODD_D2R_C_N	38 90	
TRUE	SATA_ODD_R2D_P	38 90	
TRUE	SATA_ODD_R2D_N	38 90	
TRUE	GND		5 TPs

J4501 (SATA HDD CONN)

TRUE	PP5V_S0_HDD_FLT	38
TRUE	SATA_HDD_R2D_P	38 90
TRUE	SATA_HDD_R2D_N	38 90
TRUE	SATA_HDD_D2R_C_N	38 90
TRUE	SATA_HDD_D2R_C_P	38 90
TRUE	GND	

J5815 (KBD BACKLIGHT CONN)

TRUE	KBDLED_ANODE	50
TRUE	SMC_KDBLED_PRESENT_L	50
TRUE	GND	

FUNC_TEST

TRUE	GND	
TRUE	GND	6 TPs

USB PORTS

TRUE	PP5V_S3_RTUSB_A_F	39	
TRUE	USB2_LT1_N	39 96	
TRUE	USB2_LT1_P	39 96	
TRUE	GND		
TRUE	PP5V_S3_RTUSB_B_F	39	
TRUE	USB_LT2_N	39 96	
TRUE	USB_LT2_P	39 96	
TRUE	GND		
TRUE	PP5V_S3_RTUSB_C_F	98	
TRUE	USB_LT3_N	96 98	
TRUE	USB_LT3_P	96 98	
TRUE	GND		

J3401 (AIRPORT/BT/CAMERA CONN)

TRUE	PCIE_MINI_D2R_P	17 30 90
TRUE	PCIE_MI[redacted]	
TRUE	PCIE_CL[redacted]	
TRUE	MINI_CLKREQ_Q_L	30
TRUE	PCIE_WAKE_L	7 17 30 31
TRUE	MINI_RESET_CONN_L	30
TRUE	PP5V_WLAN	30
TRUE	PP5V_S3_BTCAMERA_F	30
TRUE	SMBUS_SMC_A_S3_SDA	7 44 94
TRUE	SMBUS_SMC_A_S3_SCL	7 44 94
TRUE	USB_CAMERA_CONN_P	30 96
TRUE	USB_CAMERA_CONN_N	30 96
TRUE	CONN_USB2_BT_P	30 96
TRUE	CONN_USB2_BT_N	30 96

J3500 (EXPRESS CARD CONN)

TRUE	PP1V5_S0_EXCARD_SWITCH	31
TRUE	PCIE_WAKE_L	7 17 30 31
TRUE	SMBUS_MCP_0_CLK	13 21 44 91
TRUE	SMBUS_MCP_0_DATA	13 21 44 91
TRUE	PP3V3_S0_EXCARD_SWITCH	31
TRUE	PP3V3_S3_EXCARD_SWITCH	31
TRUE	USB2_EXCARD_CONN_N	31 96
TRUE	USB2_EXCARD_CONN_P	31 96
TRUE	EXCARD_C[redacted]	
TRUE	EXCARD_C[redacted]	
TRUE	EXCARD_C[redacted]	
TRUE	PLT_RESE[redacted]	
TRUE	PCIE_EXC[redacted]	
TRUE	PCIE_EXCARD_D2R_N	17 31 90
TRUE	PCIE_EXCARD_R2D_P	31 90
TRUE	PCIE_EXCARD_R2D_N	31 90
TRUE	PCIE_CLK100M_EXCARD_CONN_P	31 96
TRUE	PCIE_CLK100M_EXCARD_CONN_N	31 96

J5800 (IPD FLEX CONN)

TRUE	PP3V3_S3_LDO	50
TRUE	PP18V5_S3	7 50
TRUE	TPAD_GND_F	50
TRUE	Z2_CS_L	49 50
TRUE	Z2_DEBUG3	49 50
TRUE	Z2_MISO	49 50
TRUE	Z2_BOOST_EN	50
TRUE	Z2_BOOT_CFG1	49 50
TRUE	Z2_CLKIN	49 50
TRUE	Z2_KEY_ACT_L	49 50
TRUE	Z2_RESET	49 50
TRUE	PSOC_F_CS_L	49 50
TRUE	PICKB_L	49 50
TRUE	PSOC_MISO	49 50
TRUE	PSOC_MOSI	49 50
TRUE	PSOC_SCLK	49 50
TRUE	SMBUS_SMC_A_S3_SCL	
TRUE	SMBUS_SMC[redacted]	

J6900 (DC POWER [redacted]

TRUE	ADAPTER_S[redacted]	
TRUE	PP18V5_DCIN_FUSE	59
TRUE	GND	

J6950 (MAIN BATT CONN)

TRUE	PPVBAT_G3H_CONN_F	59
TRUE	SMBUS_SMC_BSA_SCL	7 44 94
TRUE	SMBUS_SMC_BSA_SDA	7 44 94
TRUE	SMC_BS_ALRT_L	41 42 59
TRUE	GND	

J6995 (BAT LED CONN)

TRUE	PP3V42_G3H	7 8 42
TRUE	SMBUS_SMC_BSA_SDA	7 44 94
TRUE	SMBUS_SMC_BSA_SCL	7 44 94
TRUE	SMC_BIL_BUTTON_DB_L	42 59
TRUE	GND	

J5713 (KEY BOARD CONN)

TRUE	PP3V3_S3	7 8
TRUE	PP3V42_G3H	7 8 42
TRUE	WS_KBD1	49
TRUE	WS_KBD2	49
TRUE	WS_KBD3	49
TRUE	WS_KBD4	49
TRUE	WS_KBD5	49
TRUE	WS_KBD6	49
TRUE	WS_KBD7	49
TRUE	WS_KBD8	49
TRUE	WS_KBD9	49
TRUE	WS_KBD10	49
TRUE	WS_KBD11	49
TRUE	WS_KBD12	49
TRUE	WS_KBD13	49
TRUE	WS_KBD14	49
TRUE	WS_KBD15_CAP	49
TRUE	WS_KBD16_NUM	49
TRUE	WS_KBD17	49
TRUE	WS_KBD18	49
TRUE	[redacted]	
TRUE	WS_K[redacted]FF_L	
TRUE	WS_LEFT_SHIFT_KBD	49
TRUE	WS_LEFT_OPTION_KBD	49
TRUE	WS_CONTROL_KBD	49

J4800 (FRONT CABLE CONN)

TRUE	PP3V42_G3H_LIDSWITCH_R	40
TRUE	PP5V_S3_IR_R	40
TRUE	SMC_LID_R	40
TRUE	IR_RX_OUT	40
TRUE	SYS_LED_ANODE	40 42
TRUE	GND	

J5502 (SENSOR CONN)

TRUE	MCPTHMSNS_D_P	47 96
TRUE	MCPTHMSNS_D_N	47 96

FUNC_TEST

TRUE	SYS_LED_ANODE_R	40
TRUE	LPC_CLK33M_LPCPLUS	25 43 91
TRUE	LPC_AD<0..3>	19 41 43 84 91
TRUE	SPI_ALT_MOSI	43
TRUE	SPI_ALT_MISO	43
TRUE	LPC_FRAME_L	19 41 43 84 91
TRUE	PM_CLKRUN_L	19 41 43
TRUE	SMC_TMS	41 42 43
TRUE	DEBUG_RESET_L	25 43
TRUE	SMC_TDO	41 42 43
TRUE	SMC_TRST_L	41 43
TRUE	SMC_MD1	41 43
TRUE	SMC_TX_L	39 41 42 43
TRUE	SPIROM_USE_MLB	43
TRUE	SPI_ALT_CLK	43
TRUE	SPI_ALT_CS_L	43
TRUE	LPC_SERIRQ	19 41 43
TRUE	LPC_PWRDWN_L	19 41 43
TRUE	SM[redacted]	
TRUE	[redacted]	41 42 43
TRUE	[redacted]	
TRUE	[redacted]	
TRUE	[redacted]

"G3Hot" (Always-Present) Rails

60 =PPBUS_G3H — PPBUS_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=6V
MAKE_BASE=TRUE
- =PPVIN_S5_P5VP3V3 — 62
- =PPVIN_S0_CPUVTTS0 — 65
- =PPBUS_S0_LCDBKLT — 86
- =PPVIN_GPU_GPUVCORE — 77
- =PPVIN_S5_CPU_IMVP_ISNS_R — 45
- =PPVIN_S0_P5VRTS0_MCPCORE — 64
- =PPVIN_S3_DDRREG — 63
- =PPVIN_S0GPU_P1V8P1V1 — 83
- =PPVBAT_G3H_P3V42G3H — 59
- =PPVIN_S0_P1V05S5 — 66
- =PPVIN_PBUS_KBDLED — 9
- =PPVIN_S5_FWPWRSW — 36
- =PPVIN_S5_BKL

45 =PPVIN_S5_CPU_IMVP_ISNS — PPBUS_CPU_IMVP_ISNS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=6V
MAKE_BASE=TRUE
- =PPVIN_S5_CPU_IMVP — 61

59 =PP18V5_DCIN_CONN — PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
- =PPDCIN_S5_CHGR — 60

59 =PP3V42_G3H_REG — PP3V42_G3H
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
- =PP3V42_G3H_SMCUSBMUX — 39
- =PP3V42_G3H_SMBUS_SMC_BSA — 44
- =PP3V42_G3H_LIDSWITCH — 40
- =PP3V3_S5_SMC — 41 42 51
- =PP3V3_S5_LPCPLUS — 43
- =PPVIN_S5_SMCVREF — 42
- =PP3V42_G3H_PWRCTL — 67
- =PP3V42_G3H_CHGR — 60
- =PP3V3_S5_RTC_D — 25
- =PP3V42_G3H_BATT — [illegible]
- =PP3V42_G3H_TPAD — [illegible]
- =PP3V42_G3H_BMON_ISNS — [illegible]
- =PP3V42_G3H_CPUCOREISNS — [illegible]

5V Rails

62 =PP5V_S3_REG — PP5V_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S3_SYSLED — 42
- =PP5V_S3_BTCAMERA — 30
- =PP5V_S3_WLAN — 30
- =PP5V_S3_IR — 40
- =PP5V_S3_DDRREG — 63
- =PP5V_S3_GPUVCORE — 77
- =PP5V_S3_RTUSB — 39 98
- =PP5V_S3_TPAD — 50
- =PP5V_S3_P1V05S0FET — 68
- =PP5V_S3_MCPDDRFET — 68
- =PP5V_S3_VTTCLAMP — 68
- =PP5V_S3_AUDIO_PWR — 9

64 =PP5V_S0_REG — PP5V_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S0_FAN_LT — 7 48
- =PP5V_S0_FAN_RT
- =PP5V_S0_CPU_IMVP
- =PP5V_S0_CPUVTTS0
- =PP5V_S0GPU_P1V1P1V8_GPU
- =PP5V_S0_LPCPLUS
- =PP5V_S0_ODD — 38
- =PP5V_S0_HDD — 38
- =PPVIN_PP5V_KBDLED — 9

Chipset "VCore" Rails

61 =PPVCORE_S0_CPU_REG — PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU — 11 12 45

64 =PPMCPCORE_S0_REG — PPVCORE_S0_MCP
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PPVCORE_S0_MCP — 22 23 45

3.3V-2.5V Rails

62 =PP3V3_S5_REG — PP3V3_S5
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_S5_ROM — 43 52
- =PP3V3_S5_MEMRESET — 29
- =PP3V3_S3_P3V3S3FET — 68
- =PP3V3_S0_LCD — 78
- =PP3V3_S0_P3V3S0FET — 68
- =PP3V3_GPU_P3V3GPUFET — 68
- =PP3V3_S5_PWRCTL — 67
- =PP3V3_S5_P1V05FET — 68
- =PP3V3_S5_MCP — 22 23
- =PP3V3_S5_MCP_GPIO — 18 20
- =PP3V3_FW_LATEVG_ACTIVE — 36
- =PP3V3_S5_MCPPWRGD — 25
- =PP3V3_FW_LATEVG — 37
- =PP3V3_S5_P1V05ENETFET — [illegible]
- =PP[illegible]_S5_P3V3ENETFET — [illegible]
- [illegible]
- =PP3V3_S3_GMUX — 84
- =PP3V3_S3_BT — 30
- =PP3V3_S3_P1V8S0 — 66
- =PP3V3_S3_SMBUS_SMC_A_S3 — 44
- =PP3V3_S3_SMS — 8 51
- =PP3V3_S3_TPAD — 49
- =PP3V3_S3_SMS — 8 51
- =PP3V3_S3_WLAN — 30
- =PP3V3_S3_MCP_GPIO — 21
- =PP3V3_S3_VREFMRGN — 26
- =PP3V3_S3_SMBUS_SMC_MGMT — 44
- =PP3V3_S3_EXCARD — 31
- =PP3V3_S3_P1V5EXPS0 — 66

68 =PP3V3_S0_FET — PP3V3_S0
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP[illegible]_S0_LPCPLUS — [illegible]
- =PP[illegible]_S0_SMC — [illegible]
- [illegible]
- =PP3V3_S0_FAN_LT — 48
- =PP3V3_S0_FAN_RT — 48
- =PP3V3_S0_IMVP — 61
- =PP3V3_S0_PWRCTL — 67
- =PP3V3_S0_DDC_LCD — 7 75 78
- =PP3V3_S0_XDP — 6 8 13
- =PP3V3_S0_MCPCOREISNS — 46
- =PP3V3_S0_XDP — 6 8 13
- =PPSPD_S0_MEM_A — 27
- =PPSPD_S0_MEM_B — 28
- =PP3V3_S0_SMBUS_MCP_0 — 44
- =PP3V3_S0_GMUX — 84
- =PP3V3_S0_DPMUX — 81
- =PP3V3_S0_DPCONN — 82
- =PP3V3_S0_P1V2P2V5 — 87
- =PP3V3_S0_MCP_GPIO — 18 19 21
- =PP3V3_S0_HDCPROM — 24
- =PP3V3R1V5_S0_MCP_HDA — 21 23
- =PP3V3_S0_MCP_PLL_UF — 23
- =PP3V3_S0_MCP_VPLL_UF — 24
- =PP3V[illegible]_S0_MCP_DAC_UF — 24
- =PP3V[illegible]_MCP — 21
- [illegible]
- =PP[illegible]V3_S0_EXCARD — 31
- =PP[illegible]V3_S0_LVDSDDC[illegible] — 81
- =PP3V3_S0_BATTCHARGERTMPSNSR — 47
- =PP3V3_GPU_SMBUS_SMC_0_S0 — 44
- =PP3V3_S0_TPAD — 50
- =PP3V3_S0_MCP_PLL_VLDO — 66
- =PP3V3_FW_FWPHY — 35 37
- =PP3V3_FW_P1V0FW — 66

87 =PP2V5_S0_REG — PP2V5_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=2.5V
MAKE_BASE=TRUE
- =PP2V5_S0_GMUX — 84

87 =PP1V2_S0_REG — PP1V2_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE
- =PP1V2_S0_GMUX — 84

1.8V/DDR 1.5V Rails

66 =PP1V8_S0_REG — PP1V8_S0
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
500 mA max supply
- 190 mA =PP3V3R1V8_S0_MCP_IFP_VDD — 18 24
- =PP1V8_S0_MCP_PLL_VLDO — 66

63 =PPDDR_S3_REG — PP1V8R1V5_S3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V8R1V5_S0_MCP_FET — 68
- =PPVIN_S0_DDRREG_LDO — 63
- =PP1V5_S3_MEM_A — 27
- =PP1V5_S3_MEM_B — 28
- =PP1V5_S3_MEMRESET — 29

68 =PP1V8R1V5_S0_FET — PP1V8R1V5_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PPMCPDDR_ISNS_R — 46
- [illegible]
- [illegible] — 11 12
- [illegible] — 67
- [illegible]
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S0_EXCARD — 31

23 16 =PP1V8R1V5_S0_MCP_MEM — PPMCPDDR_ISNS
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S0_MEM_A — 27
- =PP1V5_S0_MEM_B — 28
- =PPMCPDDR_ISNS — 46

68 66 =PP1V05_S0_FET — PP1V05_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0_MCP_AVDD_UF — 23
- =PP1V05_S0_MCP_PEX_DVDD — 8 23
- =PP1V05_S0_MCP_SATA_DVDD — 8 23
- =PP1V05_S0_MCP_HDMI_VDD — 18 24
- =PP1V05_S0_VMON — 67
- =PP1V05_S0_MCP_PLL_PEX_UF — 23

1034 mA
- [illegible] — 23 66
- [illegible] — 17
- [illegible] — 17

23 =PP1V05_S0_MCP_PEX_AVDD — MAKE_BASE=TRUE
- =PP1V05_S0_MCP_PEX_AVDD0 — 17
- =PP1V05_S0_MCP_PEX_AVDD1 — 17

23 8 =PP1V05_S0_MCP_SATA_DVDD
- =PP1V05_S0_MCP_SATA_DVDD0 — 20

23 =PP1V05_S0_MCP_SATA_AVDD — MAKE_BASE=TRUE
- =PP1V05_S0_MCP_SATA_AVDD0 — 20

66 =PP1V05_S5_MCP — PP1V2R1V05_S5
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
(1.1V for A01) — 7
241 mA max load
- 105 mA/241 mA =PP1V05_S5_MCP_VDD_AUXC — 22 23
- 139 mA/ 0 mA =PP1V05_ENET_P1V05ENETFET — 33
- =PP1V05_S5_P1V05S0FET — 68

65 =PPCPUVTT_S0_REG — PPCPUVTT_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
5300 mA — 7
- 4500 mA =PP1V05_S0_CPU — 6 10 11 12 13 61
- =PP1V05_S0_SMC_LS — 42
- 1182 mA =PP1V05_S0_MCP_FSB — 9 14 22 23

26 =PPVTT_S3_DDR_BUF — PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
- [illegible] — 7
- [illegible]
- [illegible]
- [illegible]
- [illegible]
- =PP0V75_S0_MEM_VTT_A — 27
- =PP0V75_S0_MEM_VTT_B — 28
- =PPVTT_S0_VTTCLAMP — 68

OR 0.75V

ENET Rails

33 =PP1V05_ENET_FET — PP1V2R1V05_ENET
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE — 7
- =PP1V05_ENET_MCP_PLL_MAC — 23
- =PP1V05_ENET_MCP_RMGT — 18 23
- =PP1V05_ENET_PHY — 32

33 =PP3V3_ENET_FET — PP3V3_ENET_PHY
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE — 7
- =PP3V3_ENET_MCP_RMGT — 18 23
- =PP3V3_ENET_PHY — 32

"FW" (FireWire) Rails

36 =PPVOUT_FW_FWPWRSW — PPBUS_FW_FWBOOST
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=6V
MAKE_BASE=TRUE
- =PPVIN_PFWBOOST — 66

66 =PFWBOOST_REG — PP10V_FW
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=10V
MAKE_BASE=TRUE
- =PPBOOST_FW_FWPWRSW_F — 36

36 =PPBOOST_S5_FW_FET — PPVP_FW
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=10V
MAKE_BASE=TRUE — 7
- =PPVP_FW_PORT1 — 37
- =PPVP_FW_PHY_CPS_FET — 37

66 =PP1V0_FW_REG — PP1V0_FW
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
MAKE_BASE=TRUE — 7
- =PP1V0_FW_FWPHY — 35

"GPU" Rails

68 =PP3V3_S0GPU_FET — PP3V3_S0GPU
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE — 7
- =PP3V3_GPU_VDD33 — 6 74 75
- =PP3V3_GPU_MIO — 74 75
- =PP3V3_GPU_LVDS_DDC — 81
- =PP3V3_GPU_PWRCTL — 67
- =PP3V3_GPU_VCORELOGIC — 77
- =PP3V3_GPU_P1V8S0 — 66

83 =PP1V1_S0GPU_REG — PP1V1_S0GPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.1V
MAKE_BASE=TRUE — 7
- =PP1V1_GPU_PEX_IOVDDQ — 69
- =PP1V1_GPU_PEX_IOVDD — 69
- =PP1V1_GPU_PEX_PLLXVDD — 69
- =PP1V1_GPU_PLLVDD — 74
- =PP1V1_GPU_H_PLLVDD — 74
- =PP1V1_GPU_VID_PLLVDD — 74
- =PP1V1_GPU_FBPLLAVDD — 71
- =PP1V1_GPU_IFPCD_IOVDD — 76

66 =PP1V8_GPUIFPX_REG — PP1V8_GPUIFPX
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE — 7
- =PP1V8_GPU_IFPX — 76

46 =PP1V8_S0GPU_ISNS — PP1V8_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE — 7
- =PP1V8_GPU_FB_VDD — 72 73 79 80
- =PP1V8_GPU_FB_VDDQ — 9 72 73 79 80
- =PP1V8_GPU_FBVDDQ — 70
- =PP1V8_GPU_FBIO — 71

77 45 =PPVCORE_GPU_REG — PPVCORE_GPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE — 7
- =PPVCORE_GPU — 70

83 =PP1V8_GPU_REG — PP1V8_S0GPU_ISNS_R
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE — 7
- =PP1V8_S0GPU_ISNS_R — 46

Power Aliases

SYNC_MASTER=RXU_K20 SYNC_DATE=05/07/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 8 OF 98	

Thermal Module Holes

ZT0982 STDOFF-4.50D.98H-1.1-3.48-TH — Left CPU TM Hole
ZT0983 STDOFF-4.50D.98H-1.1-3.48-TH — Right CPU TM Hole
ZT0984 STDOFF-4.50D.98H-1.1-3.48-TH — Top GPU Right TM Hole
ZT0980 STDOFF-4.50D.98H-1.1-3.48-TH — Bottom Left GPU TM Hole
ZT0987 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0981 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0985 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0986 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0930 STDOFF-4.50D.98H-1.1-3.48-TH

Frame Holes

ZT0915 3R2P5 — GND_BATT_CHGND
ZT0945 3R2P5 — GND_CHASSIS_USB
ZT0932 3R2P5 — GND_CHASSIS_RIGHTHS
ZT0960 3R2P5 — GND_CHASSIS_SATA
ZT0971 3R2P5 — GND_CHASSIS_TPAD
ZT0965 3R2P5 — GND_CHASSIS_CLUTCH
ZT0940 3R2P5 — GND_CHASSIS_LVDS
ZT0970 3R2P5 — GND_CHASSIS_DIMM

Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa

80 79 73 72 8 =PP1V8_GPU_FB_VDDQ
R0900 10 1% 1/16W MF-LF 402 — GPU_FB_A_VREF_DIV — =PP1V8_GPU_FB_VREF_A
R0901 10 1% 1/16W MF-LF 402 — GPU_FB_B_VREF_DIV — =PP1V8_GPU_FB_VREF_B

23 22 14 8 =PP1V05_S0_MCP_FSB
NO STUFF R0970 200 5% 1/16W MF-LF 402
NO STUFF R0950 220 5% 1/10W MF-LF 402
NO STUFF R0960 62 5% 1/16W MF-LF 402
NO STUFF R0980 150 1% 1/16W MF-LF 402

88 61 14 10 OUT CPU_DPRSTP_L
88 14 10 OUT FSB_BREQ0_L
88 14 13 10 OUT FSB_CPURST_L
88 14 10 OUT CPU_INTR
88 14 10 OUT CPU_NMI

Bosses for Flex Protector Bracket

ZT0934 STDOFF-4.00D3.0H-SM
ZT0931 STDOFF-4.00D3.0H-SM
ZT0957 4.0OD1.65H-M1.6X0.35
ZT0958 4.0OD1.65H-M1.6X0.35

ZT0988 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0989 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0991 STDOFF-4.50D.98H-1.1-3.48-TH

8 =PPVIN_PBUS_KBDLED — KBDLED_PBUS R0998 0 5% 1/10W MF-LF 603 — PP5VR8V4_KBDLED (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=8.4V, MAKE_BASE=TRUE) — =PPVIN_S0_KBDLED 50
8 =PPVIN_PP5V_KBDLED — KBDLED_5V R0999 0 5% 1/10W MF-LF 603

SH0902 2.0DIA-TALL-EMI-MLB-M97-M98
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98
SH0901 2.0DIA-TALL-EMI-MLB-M97-M98
SH0920 4DIA-SHORT-EMI-MLB-M97-
SH0910 1.4DIA-EMI-MLB-M97-M98
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0923 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0916 2.0DIA-TALL-EMI-MLB-M97-M98
SH0917 2.0DIA-TALL-EMI-MLB-M97-M98
SH0918 2.0DIA-TALL-EMI-MLB-M97-M98
SH0919 2.0DIA-TALL-EMI-MLB-M97-M98
SH0930 2.0DIA-TALL-EMI-MLB-M97-M98
SH0921 2.0DIA-TALL-EMI-MLB-M97-M98
SH0922 2.0DIA-TALL-EMI-MLB-M97-M98
SH0932 2.0DIA-TALL-EMI-MLB-M97-M98
SH0934 2.0DIA-TALL-EMI-MLB-M97-M98
SH0933 2.0DIA-TALL-EMI-MLB-M97-M98
SH0935 2.0DIA-TALL-EMI-MLB-M97-M98

=PP1V05_S0_MCP_SATA_DVDD1 20
=PP1V05_S0_MCP_SATA_AVDD1 20

CPU signals

TP_IMVP6_CLKEN_L — VR_PWRGD_CLKEN_L 61
88 11 CPU_VID<0..6> — IMVP6_VID<0..6> 61 88
88 10 CPU_BSEL<0..2> — =MCP_BSEL<0..2> 14
25 MEM_VTT_EN — =DDRVTT_EN 63 68
TP_SPI_CS1_R_L_USE_MLB — =SPI_CS1_R_L_USE_MLB 21 43

GPU signals

90 69 PEG_D2R_P<0..15> — =PEG_D2R_P<0..15> 17
90 69 PEG_D2R_N<0..15> — =PEG_D2R_N<0..15> 17
90 69 PEG_R2D_C_P<0..15> — =PEG_R2D_C_P<0..15> 17
90 69 PEG_R2D_C_N<0..15> — =PEG_R2D_C_N<0..15> 17
ON 86
90 81 DP_IG_ML_P<3> — =MCP_HDMI_TXC_P 18
90 81 DP_IG_ML_N<3> — =MCP_HDMI_TXC_N 18
90 81 DP_IG_ML_P<2..0> — =MCP_HDMI_TXD_P<0..2> 18
90 81 DP_IG_ML_N<2..0> — =MCP_HDMI_TXD_N<0..2> 18
81 75 DP_IG_DDC_CLK — =MCP_HDMI_DDC_CLK 18
81 75 DP_IG_DDC_DATA — =MCP_HDMI_DDC_DATA 18
81 DP_IG_HPD — =MCP_HDMI_HPD 18

GMUX ALIASES

67 PM_ALL_GPU_PGOOD — ALL_EG_PGOOD 84
TP_LVDS_MUX_SEL_EG — LVDS_MUX_SEL_EG 84
84 EG_RESET_L — GPU_RESET_L 69
84 6 JTAG_GMUX_TDI — GMUX_JTAG_TDI 19
84 6 JTAG_GMUX_TMS — GMUX_JTAG_TMS 19
GMUX_JTAG_TDO 17
=DVI_HPD_GMUX_INT 18
IG_BKLT_EN 84
IG_LCD_PWR_EN 84

7 TP_USB_EXTDP — USB_EXTD_P 20 91
7 TP_USB_EXTDN — USB_EXTD_N 20 91
7 TP_USB_MINIP — USB_MINI_P 20 91
7 TP_USB_MININ — USB_MINI_N 20 91
7 TP_MEM_A_A<15> — MEM_A_A<15> 27
7 TP_MEM_B_A<15> — MEM_B_A<15> 28
7 TP_CPU_PECI_MCP — CPU_PECI_MCP 14
7 TP_LVDS_IG_B_CLKP — LVDS_IG_B_CLK_P 18 90
7 TP_LVDS_IG_B_CLKN — LVDS_IG_B_CLK_N 18 90
7 TP_LVDS_IG_BKL_PWM — LVDS_IG_BKL_PWM 18

NC_LVDS_IG_A_DATAP<3> — LVDS_IG_A_DATA_P<3> 18 90
NC_LVDS_IG_A_DATAN<3> — LVDS_IG_A_DATA_N<3> 18 90
NC_LVDS_IG_B_DATAP<3> — LVDS_IG_B_DATA_P<3> 18 90
NC_LVDS_IG_B_DATAN<3> — LVDS_IG_B_DATA_N<3> 18 90

AUDIO ALIASES

53 HDA_BITCLK — HDA_BIT_CLK 21 91
8 =PP5V_S3_AUDIO_PWR — XW0900 SM — PP5V_S3_AUDIO (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V) 53 55
XW0901 SM — PP5V_S3_AUDIO_AMP (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V) 56
R0902 10K 5% 1/16W MF-LF 402 — AUD_IPHS_SWITCH_EN 19 58

R0903 0 5% 1/16W MF-LF 402
21 MCP_SPKR — SMC_MCP_SAFE_MODE 41

ETHERNET ALIASES

33 =P3V3ENET_EN — PM_SLP_RMGT_L 21
33 =P1V05ENET_EN
32 =PP3V3_ENET_PHY_VDDREG — TP_PP3V3_ENET_PHY_VDDREG
32 =RTL8211_REGOUT — NC_RTL8211_REGOUT
=RTL8211_ENSWREG 32

MCP79 PCIe PRSNT# Straps

R0925 0 5% 1/16W MF-LF 402 — PCIE_FW_PRSNT_L — OUT 17
NO STUFF R0927 0 5% 1/10W MF-LF 402 — PEG_PRSNT_L — OUT 17
R0926 0 5% 1/16W MF-LF 402 — EG_CLKREQ_OUT_L — IN 84

MCP_MII_PD
R0930 47K 5% 1/16W MF-LF 402
=MCP_MII_RXER 18
=MCP_MII_CRS 18
=MCP_MII_COL 18

Digital Ground

GND (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=0V)

Signal Aliases

SYNC_MASTER=K20_MLB — SYNC_DATE=09/24/2008

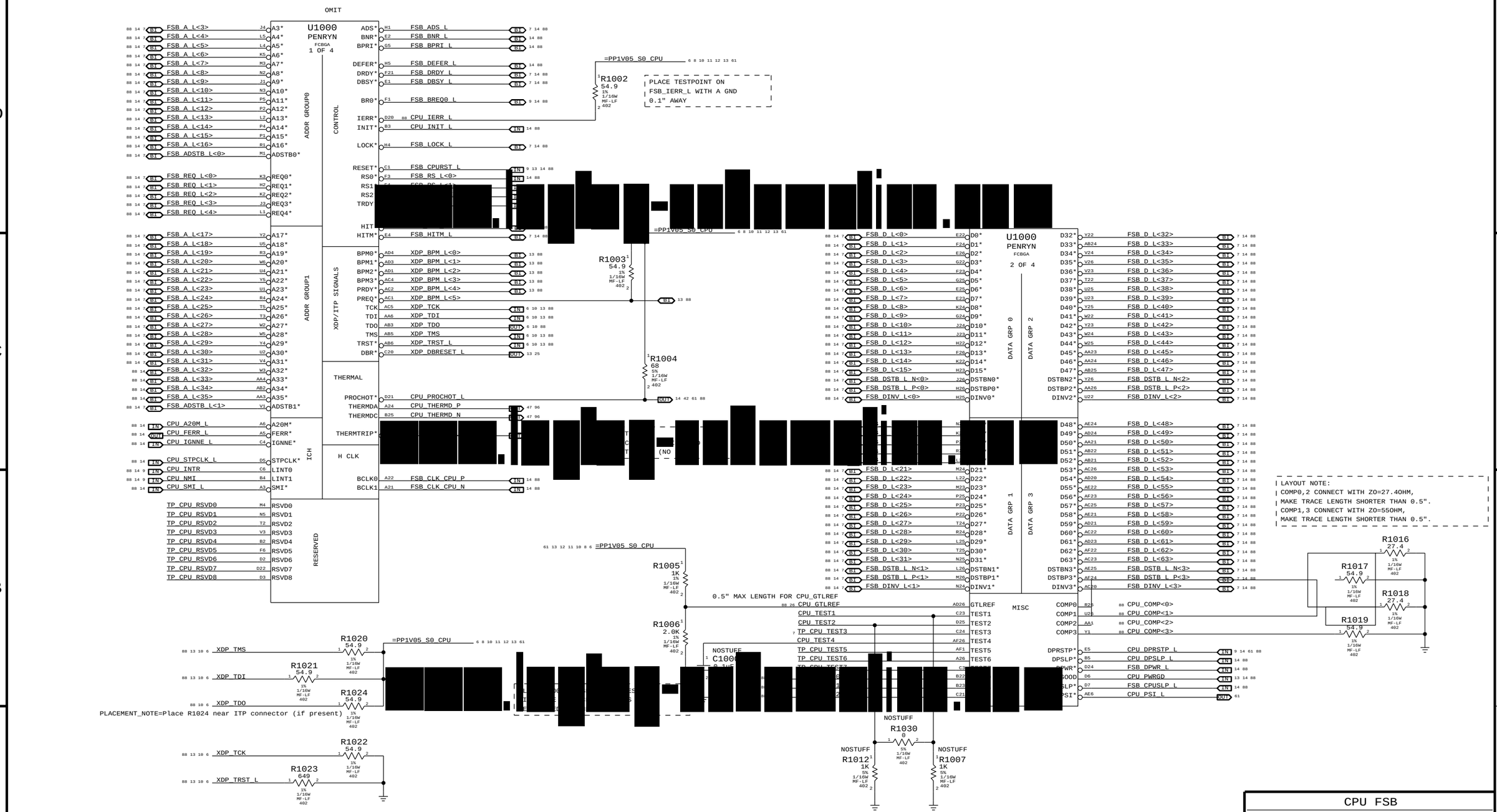
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 9 OF 98	



CPU FSB

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

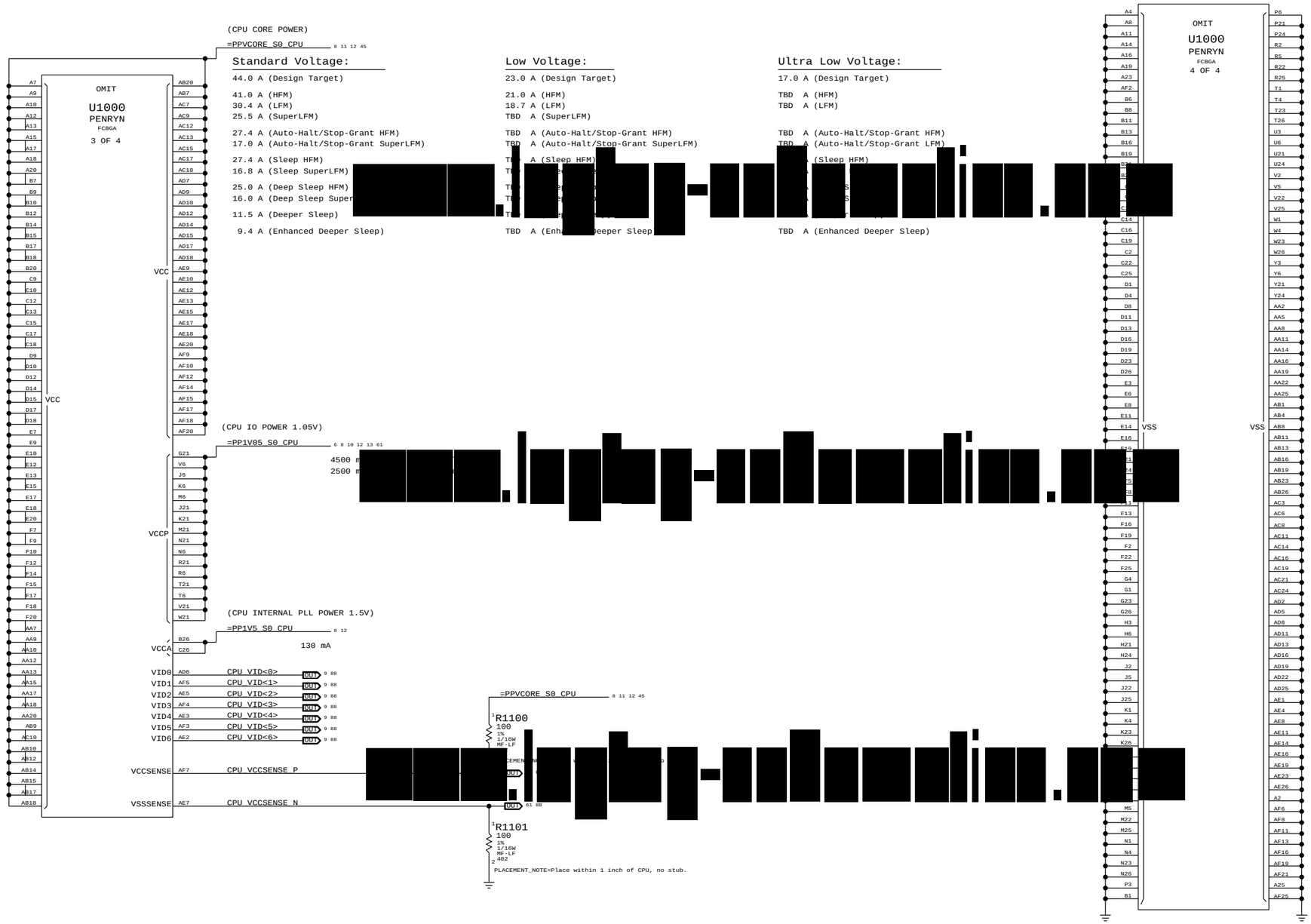
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 10 OF 98



Current numbers from Merom for Santa Rosa EMTS, doc #22221.

CPU Power & Ground

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

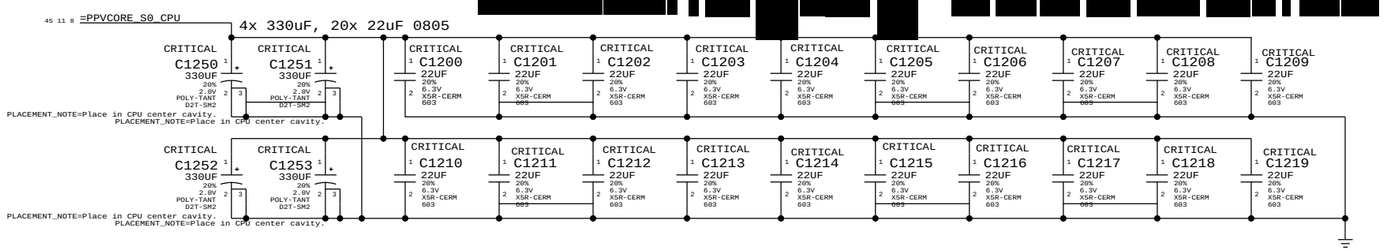
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

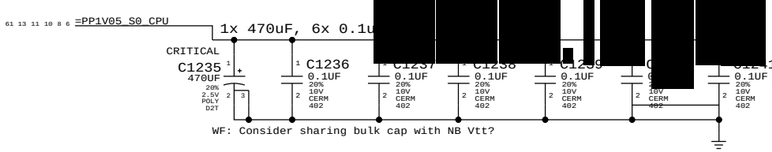
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 11 OF 98	

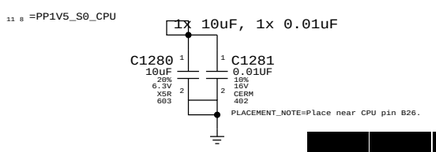
CPU V[redacted]BU[redacted]



VCCP (CPU I/O) DECOUPLING [redacted]



VCCA (CPU AVdd) DECOUPLING



[redacted]

CPU Decoupling & VID

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

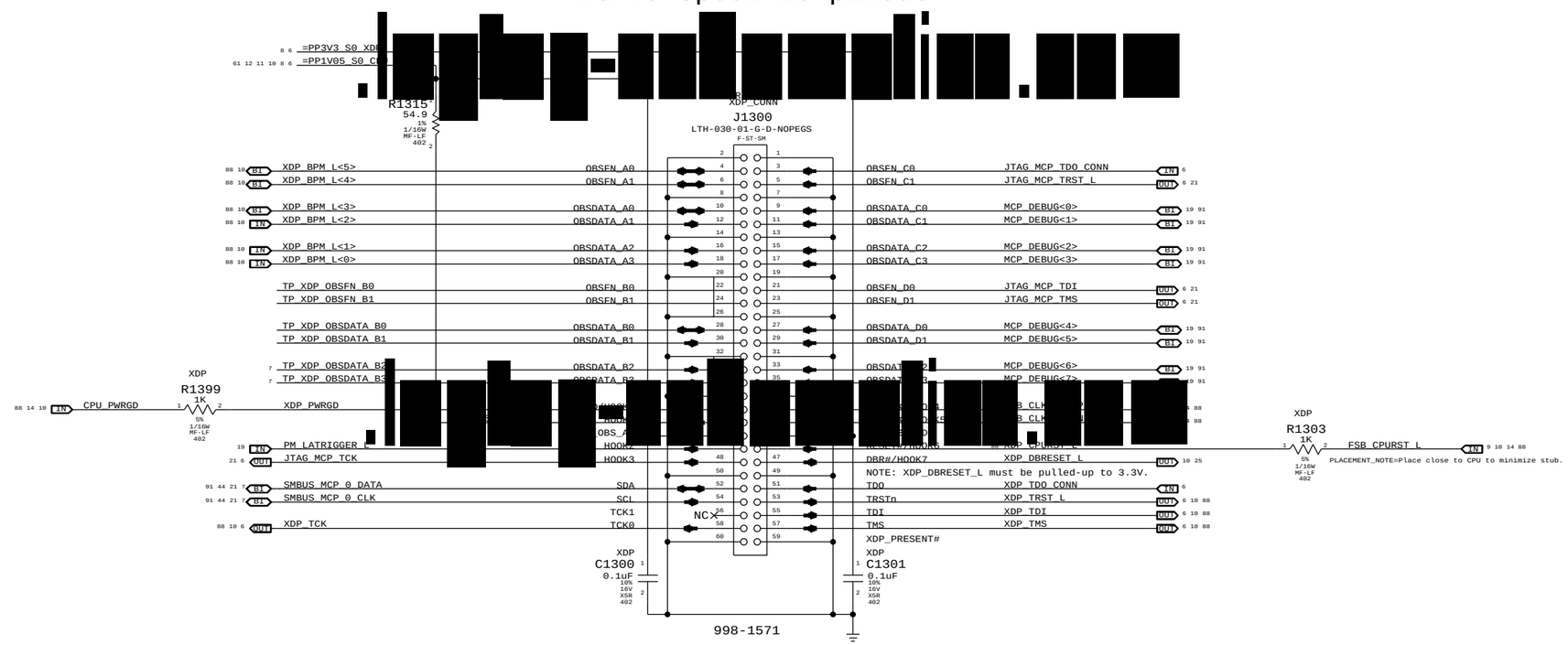
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 12 OF 98	

Mini-XDP Connector

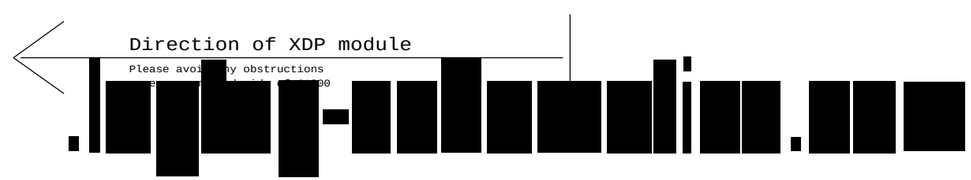
NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



NOTE: XDP_DBRESET_L must be pulled-up to 3.3V.



eXtended Debug Port(MiniXDP)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

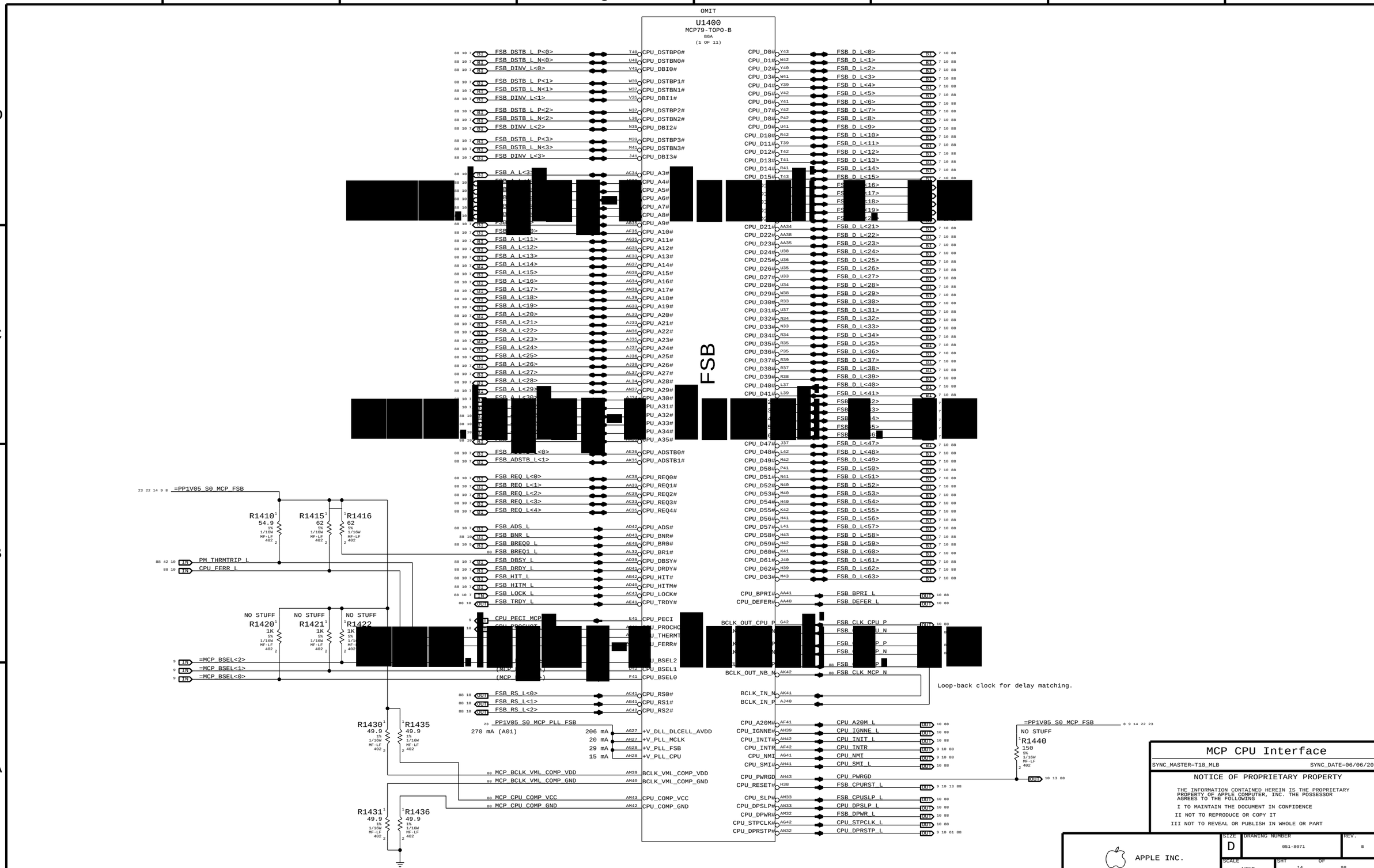
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

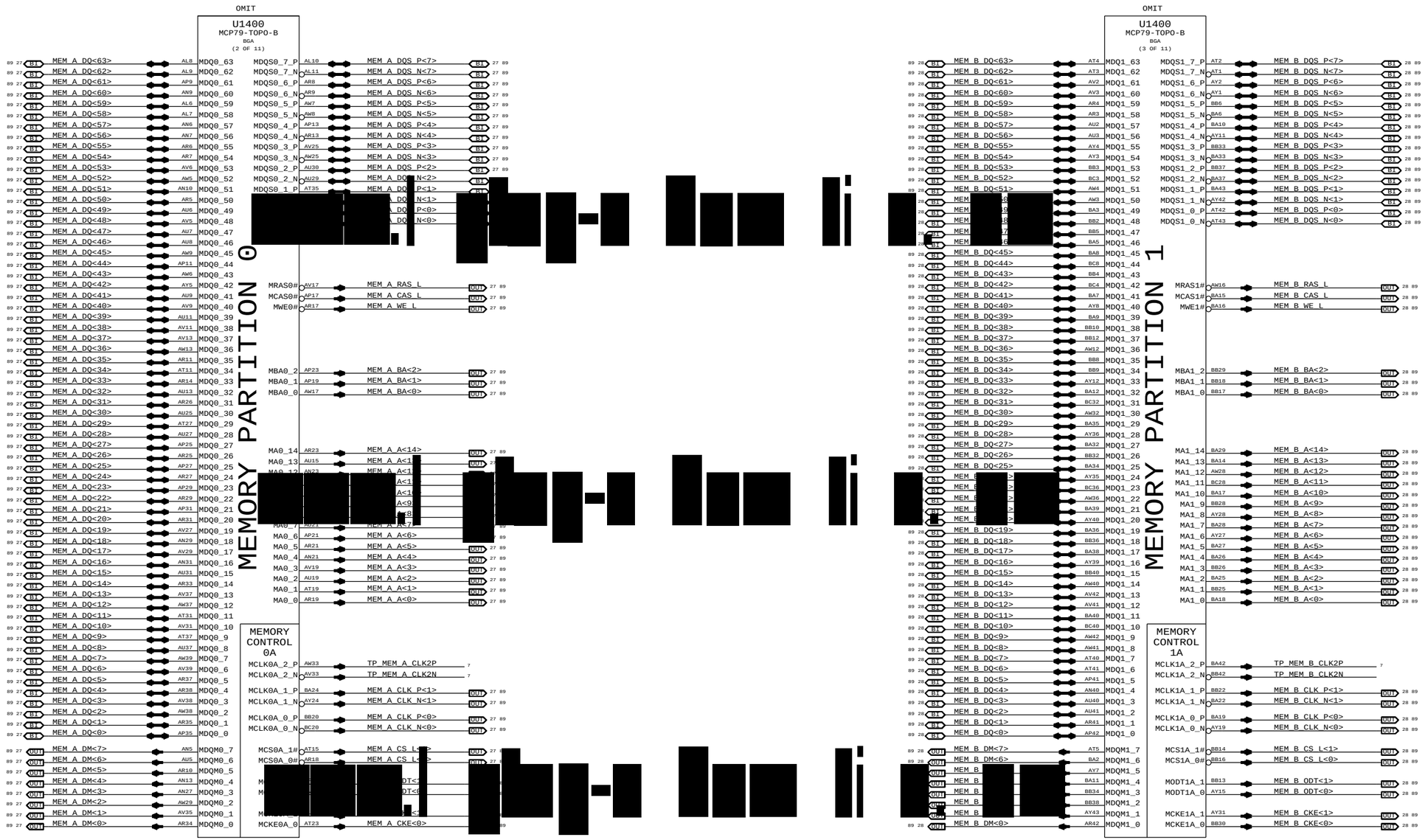
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 13 OF 98	



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



MCP Memory Interface

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

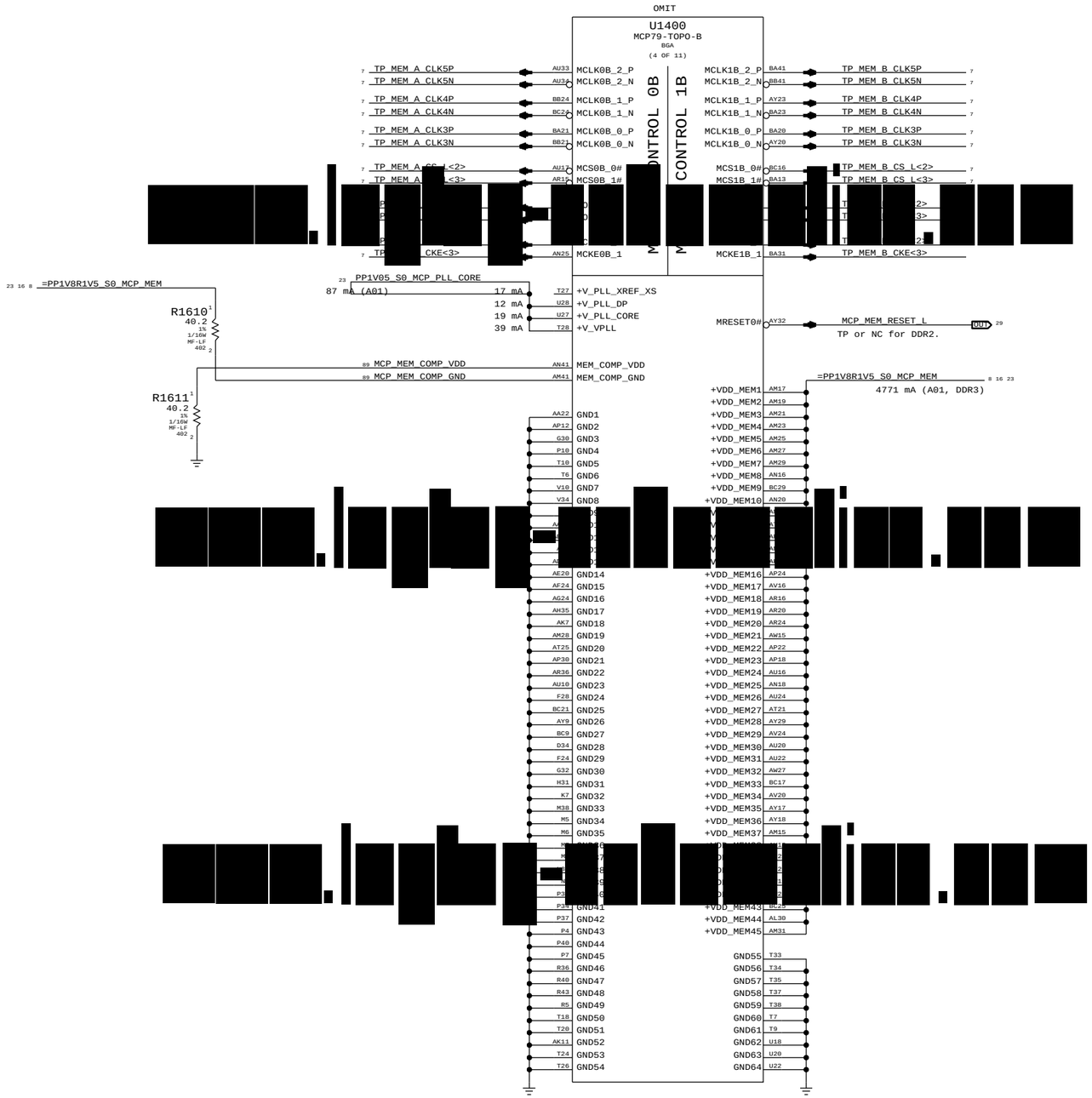
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 15 OF 98	



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 16 OF 98

OMIT

U1400
MCP79-TOPO-B
BGA
(5 OF 11)

PCI EXPRESS

Signal	Pin	Dir
=PEG_D2R_P<0>	F7 PE0_RX0_P	IN
=PEG_D2R_N<0>	E7 PE0_RX0_N	IN
=PEG_D2R_P<1>	D7 PE0_RX1_P	IN
=PEG_D2R_N<1>	C7 PE0_RX1_N	IN
=PEG_D2R_P<2>	E6 PE0_RX2_P	IN
=PEG_D2R_N<2>	E6 PE0_RX2_N	IN
=PEG_D2R_P<3>	E5 PE0_RX3_P	IN
=PEG_D2R_N<3>	F5 PE0_RX3_N	IN
=PEG_D2R_P<4>	E4 PE0_RX4_P	IN
=PEG_D2R_N<4>	E3 PE0_RX4_N	IN
=PEG_D2R_P<5>	C3 PE0_RX5_P	IN
=PEG_D2R_N<5>	D3 PE0_RX5_N	IN
=PEG_D2R_P<6>	G5 PE0_RX6_P	IN
=PEG_D2R_N<6>	H5 PE0_RX6_N	IN
=PEG_D2R_P<7>	J7 PE0_RX7_P	IN
=PEG_D2R_N<7>	[illegible]	IN
=PEG_D2R_P<8>	[illegible]	IN
=PEG_D2R_N<8>	[illegible]	IN
=PEG_D2R_P<9>	[illegible]	IN
=PEG_D2R_N<9>	[illegible]	IN
=PEG_D2R_P<10>	L9 PE0_RX10_P	IN
=PEG_D2R_N<10>	L8 PE0_RX10_N	IN
=PEG_D2R_P<11>	L7 PE0_RX11_P	IN
=PEG_D2R_N<11>	L6 PE0_RX11_N	IN
=PEG_D2R_P<12>	N11 PE0_RX12_P	IN
=PEG_D2R_N<12>	N10 PE0_RX12_N	IN
=PEG_D2R_P<13>	N9 PE0_RX13_P	IN
=PEG_D2R_N<13>	P9 PE0_RX13_N	IN
=PEG_D2R_P<14>	N7 PE0_RX14_P	IN
=PEG_D2R_N<14>	M6 PE0_RX14_N	IN
=PEG_D2R_P<15>	N5 PE0_RX15_P	IN
=PEG_D2R_N<15>	M4 PE0_RX15_N	IN
PEG_PRSNT_L	C9 PE0_PRSNT_16# Int PU	IN
MINI_CLKREQ_L	D5 PEB_CLKREQ#/GPIO_49 Int PU	IN
PCIE_MINI_PRSNT_L	D9 PEB_PRSNT# Int PU	IN
FW_CLKREQ_L	E8 PEC_CLKREQ#/GPIO_50 Int PU	IN
PCIE_FW_PRSNT_L	C10 PEC_PRSNT# I[illegible]	IN
[illegible]	[illegible]	[illegible]
AUD_IP_PERIPHERAL_DET	M16 PEF_CLKREQ#/GPIO_17 Int PU	IN
GMUX_JTAG_TCK_L	M18 PEF_PRSNT#/GPIO_47 Int PU	OUT
TP_MCP_GPIO_18	M17 PEG_CLKREQ#/GPIO_18 Int PU	
GMUX_JTAG_TDO	M19 PEG_PRSNT#/GPIO_48 Int PU	IN
PCIE_WAKE_L	F17 PE_WAKE# Int PU (S5)	IN
PCIE_MINI_D2R_P	K9 PE1_RX0_P	IN
PCIE_MINI_D2R_N	J9 PE1_RX0_N	IN
PCIE_FW_D2R_P	H9 PE1_RX1_P	IN
PCIE_FW_D2R_N	G9 PE1_RX1_N	IN
PCIE_EXCARD_D2R_P	F9 PE1_RX2_P	IN
PCIE_EXCARD_D2R_N	E9 PE1_RX2_N	IN
TP_PCIE_PE4_D2RP	H7 PE1_RX3_P	
TP_PCIE_PE4_D2RN	G7 PE1_RX3_N	
=PP1V05_S0_MCP_PEX_DVDD0	T17 +DVDD0_PEX1	
57 mA (A01, DVDD0 & 1)	W19 [illegible]	
[illegible]	U17 [illegible]	
[illegible]	[illegible]	
[illegible]	W17 [illegible]	
[illegible]	W18 +DVDD0_PEX7	
[illegible]	U16 +DVDD0_PEX8	
=PP1V05_S0_MCP_PEX_DVDD1	T19 +DVDD1_PEX1	
	U19 +DVDD1_PEX2	
PP1V05_S0_MCP_PLL_PEX	T16 +V_PLL_PEX	
84 mA (A01)		
MCP_PEX_CLK_COMP	A11 PEX_CLK_COMP	

Signal	Pin	Dir
PE0_TX0_P	C5	OUT
PE0_TX0_N	D4	OUT
PE0_TX1_P	C4	OUT
PE0_TX1_N	B4	OUT
PE0_TX2_P	A4	OUT
PE0_TX2_N	A3	OUT
PE0_TX3_P	B3	OUT
PE0_TX3_N	B2	OUT
PE0_TX4_P	C1	OUT
PE0_TX4_N	D1	OUT
PE0_TX5_P	D2	OUT
PE0_TX5_N	E1	OUT
PE0_TX6_P	E2	OUT
PE0_TX6_N	F2	OUT
PE0_TX7_P	F3	OUT
[illegible]	[illegible]	[illegible]
PE0_TX10_P	H1	OUT
PE0_TX10_N	J1	OUT
PE0_TX11_P	J2	OUT
PE0_TX11_N	J3	OUT
PE0_TX12_P	K2	OUT
PE0_TX12_N	K3	OUT
PE0_TX13_P	L4	OUT
PE0_TX13_N	L3	OUT
PE0_TX14_P	M4	OUT
PE0_TX14_N	M3	OUT
PE0_TX15_P	M2	OUT
PE0_TX15_N	M1	OUT
PE0_REFCLK_P	E11	OUT
PE0_REFCLK_N	D11	OUT
PE1_REFCLK_P	G11	OUT
PE1_REFCLK_N	F11	OUT
PE2_REFCLK_P	J11	OUT
PE2_REFCLK_N	J10	OUT
[illegible]	[illegible]	[illegible]
PE5_REFCLK_P	L14	
PE5_REFCLK_N	K14	
PE6_REFCLK_P	N14	
PE6_REFCLK_N	M14	
PEX_RST0#	K11	OUT
PE1_TX0_P	D8	OUT
PE1_TX0_N	C8	OUT
PE1_TX1_P	B8	OUT
PE1_TX1_N	A8	OUT
PE1_TX2_P	A7	OUT
PE1_TX2_N	B7	OUT
PE1_TX3_P	B6	
PE1_TX3_N	C6	
+AVDD0_PEX1	Y12	
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]
+AVDD0_PEX7	N12	
+AVDD0_PEX8	T12	
+AVDD0_PEX9	U12	
+AVDD0_PEX10	AC12	
+AVDD0_PEX11	AD12	
+AVDD0_PEX12	V12	
+AVDD0_PEX13	W12	
+AVDD1_PEX1	M13	
+AVDD1_PEX2	N13	
+AVDD1_PEX3	P13	

Signal	Pin	Dir
=PEG_R2D_C_P<0>		OUT
=PEG_R2D_C_N<0>		OUT
=PEG_R2D_C_P<1>		OUT
=PEG_R2D_C_N<1>		OUT
=PEG_R2D_C_P<2>		OUT
=PEG_R2D_C_N<2>		OUT
=PEG_R2D_C_P<3>		OUT
=PEG_R2D_C_N<3>		OUT
=PEG_R2D_C_P<4>		OUT
=PEG_R2D_C_N<4>		OUT
=PEG_R2D_C_P<5>		OUT
=PEG_R2D_C_N<5>		OUT
=PEG_R2D_C_P<6>		OUT
=PEG_R2D_C_N<6>		OUT
=PEG_R2D_C_P<7>		OUT
[illegible]	[illegible]	[illegible]
=PEG_R2D_C_P<10>		OUT
=PEG_R2D_C_N<10>		OUT
=PEG_R2D_C_P<11>		OUT
=PEG_R2D_C_N<11>		OUT
=PEG_R2D_C_P<12>		OUT
=PEG_R2D_C_N<12>		OUT
=PEG_R2D_C_P<13>		OUT
=PEG_R2D_C_N<13>		OUT
=PEG_R2D_C_P<14>		OUT
=PEG_R2D_C_N<14>		OUT
=PEG_R2D_C_P<15>		OUT
=PEG_R2D_C_N<15>		OUT
PEG_CLK100M_P		OUT
PEG_CLK100M_N		OUT
PCIE_CLK100M_MINI_P		OUT
PCIE_CLK100M_MINI_N		OUT
PCIE_CLK100M_FW_P		OUT
PCIE_CLK100M_FW_N		OUT
[illegible]	[illegible]	[illegible]
TP_PCIE_CLK100M_PE5P		
TP_PCIE_CLK100M_PE5N		
TP_PCIE_CLK100M_PE6P		
TP_PCIE_CLK100M_PE6N		
PCIE_RESET_L		OUT
PCIE_MINI_R2D_C_P		OUT
PCIE_MINI_R2D_C_N		OUT
PCIE_FW_R2D_C_P		OUT
PCIE_FW_R2D_C_N		OUT
PCIE_EXCARD_R2D_C_P		OUT
PCIE_EXCARD_R2D_C_N		OUT
TP_PCIE_PE4_R2D_CP		
TP_PCIE_PE4_R2D_CN		
=PP1V05_S0_MCP_PEX_AVDD0		
206 mA (A01, AVDD0 & 1)		
[illegible]	[illegible]	[illegible]
=PP1V05_S0_MCP_PEX_AVDD1		

NO STUFF
R1710
2.37K
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 12.7mm of U1400

If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.
If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP PCIe Interfaces

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

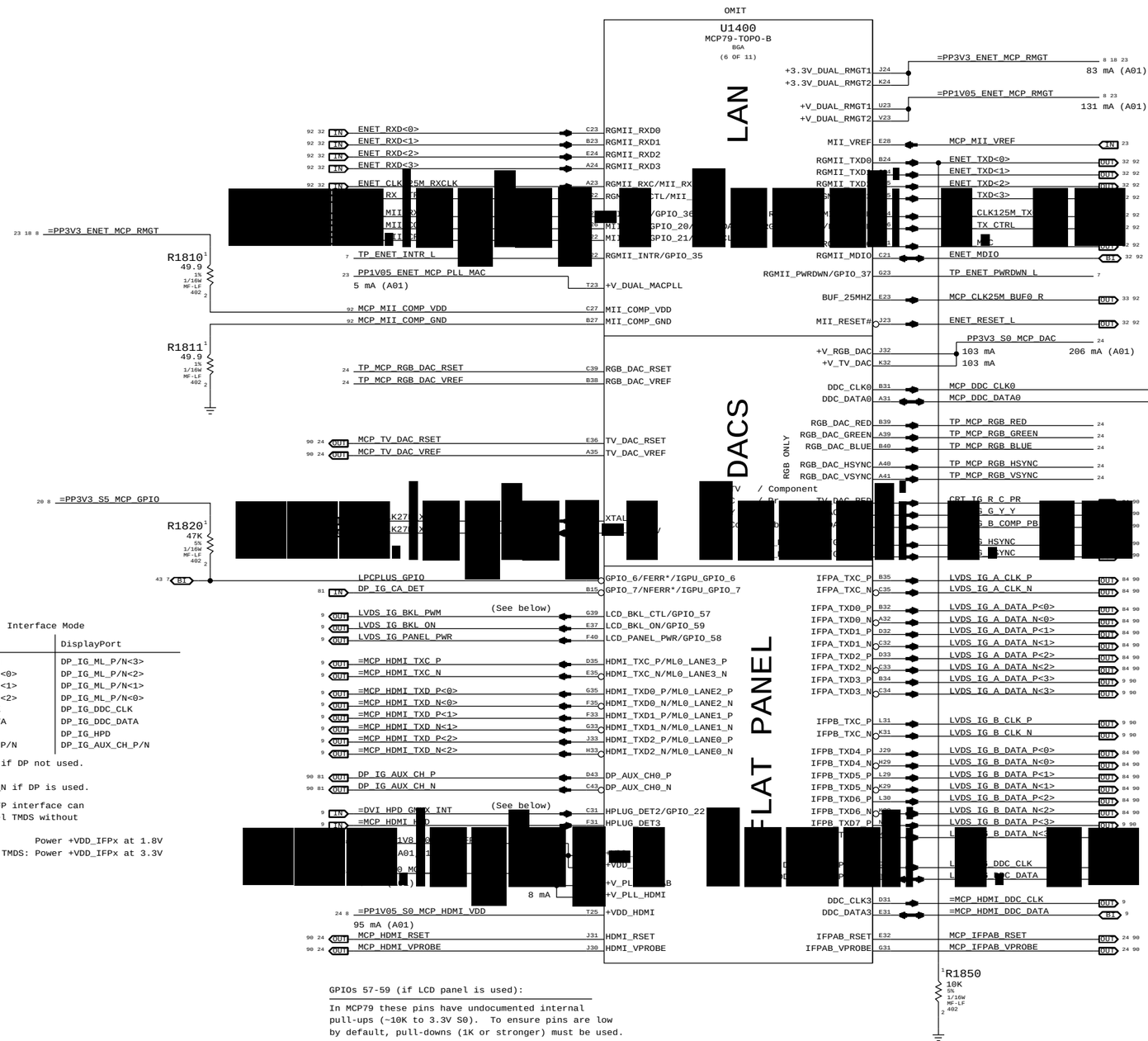
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 17 OF 98	



Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

=PP3V3_S0_MCP_GPIO

R1860 100K 5% 1/16W MF-LF 402

R1861 100K 5% 1/16W MF-LF 402

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Ethernet & Graphics

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 18 OF 98

OMIT

U1400
MCP79-TOPO-B
BGA
(7 OF 11)

PCI_REQ0 L	T2	PCI_REQ0#	
PCI_REQ1 L	V9	PCI_REQ1#/FANRPM2	
CRTMUX_SEL_TV_L	T3	PCI_REQ2#/GPIO_40/RS232_DSR#	
AUD_IPHS_SWITCH_EN	U9	PCI_REQ3#/GPIO_38/RS232_CTS#	
MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#	
MCP_DEBUG<0>	AC3	PCI_AD0	
MCP_DEBUG<1>	AE10	PCI_AD1	
MCP_DEBUG<2>	AC4	PCI_AD2	
MCP_DEBUG<3>	AE11	PCI_AD3	
MCP_DEBUG<4>	AB3	PCI_AD4	
MCP_DEBUG<5>	AC6	PCI_AD5	
MCP_DEBUG<6>	AB2	PCI_AD6	
MCP_DEBUG<7>	AC7	PCI_AD7	
TP_PCI_AD<8>	AC8	PCI_AD8	
TP_PCI_AD<9>	AA2	PCI_AD9	
TP_PCI_AD<10>	AC9	PCI_AD10	
TP_PCI_AD<11>	AC10	PCI_AD11	
TP_PCI_AD<12>	AC11	PCI_AD12	
TP_PCI_AD<13>	AA1	PCI_AD13	
TP_PCI_AD<14>	AA5	PCI_AD14	
TP_PCI_AD<15>	Y5	PCI_AD15	
TP_PCI_AD<16>	W3	PCI_AD16	
TP_PCI_AD<17>	W6	PCI_AD17	
TP_PCI_AD<18>	W4	PCI_AD18	
TP_PCI_AD<19>	W7	PCI_AD19	
TP_PCI_AD<20>	V3	PCI_AD20	
TP_PCI_AD<21>	W8	PCI_AD21	
TP_PCI_AD<22>	V2	PCI_AD22	
TP_PCI_AD<23>	W9	PCI_AD23	
TP_PCI_AD<24>	U3	PCI_AD24	
TP_PCI_AD<25>	W11	PCI_AD25	
TP_PCI_AD<26>	U2	PCI_AD26	
TP_PCI_AD<27>	U5	PCI_AD27	
TP_PCI_AD<28>	U1	PCI_AD28	
TP_PCI_AD<29>	U6	PCI_AD29	
TP_PCI_AD<30>	T5	PCI_AD30	
TP_PCI_AD<31>	U7	PCI_AD31	
TP_PCI_INTW_L	P2	PCI_INTW#	
TP_PCI_INTX_L	N3	PCI_INTX#	
TP_PCI_INTY_L	N2	PCI_INTY#	
TP_PCI_INTZ_L	N1	PCI_INTZ#	
TP_PCI_TRDY_L	Y3	PCI_TRDY#	
PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42	
FW_PME_L	AE2	LPC_DRQ1#/GPIO_19 Int PU	
TP_LPC_DRQ0_L	AE1	LPC_DRQ0# Int PU	
LPC_SERIRQ	AE6	LPC_SERIRQ Int PU	

PCI_GNT0#	R3	TP_PCI_GNT0_L	
PCI_GNT1#/FANCTL2	U10	TP_PCI_GNT1_L	
PCI_GNT2#/GPIO_41/RS232_DTR#	R4	GMUX_JTAG_TMS	OUT
PCI_GNT3#/GPIO_39/RS232_RTS#	U11	GMUX_JTAG_TDI	OUT
PCI_GNT4#/GPIO_53/RS232_SOUT#	P3	MCP_RS232_SOUT_L	OUT
PCI_CBE0#	AA3	TP_PCI_C_BE_L<0>	
PCI_CBE1#	AA6	TP_PCI_C_BE_L<1>	
PCI_CBE2#	AA11	TP_PCI_C_BE_L<2>	
PCI_CBE3#	W10	TP_PCI_C_BE_L<3>	
PCI_DEVSEL#	AA9	TP_PCI_DEVSEL_L	
PCI_[redacted]	Y4	TP_PCI_FRAME_[redacted]	
PCI_[redacted]	AA10	TP_PCI_IRDY_L	
PCI_PME#/GPIO_30	[redacted]	PM_LATRIGGER_L	OUT
PCI_RESET0#	R10	MEM_VTT_EN_R	OUT
PCI_RESET1#	R11	TP_PCI_RESET1_L	
PCI_CLK0	R6	TP_PCI_CLK0	
PCI_CLK1	R7	TP_PCI_CLK1	
PCI_CLK2	R8	PCI_CLK33M_MCP_R	
PCI_CLKIN	R9	PCI_CLK33M_MCP	
LPC_FR[redacted]	[redacted]	[redacted]	
LPC_RES[redacted]	[redacted]	[redacted]	
LPC_AD0	AD3	LPC_AD_R<0>	
LPC_AD1	AD2	LPC_AD_R<1>	
LPC_AD2	AD1	LPC_AD_R<2>	
LPC_AD3	AD5	LPC_AD_R<3>	
LPC_CLK0	AE9	LPC_CLK33M_SMC_R	OUT

Int PU (S5)

R1910 22 5% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to pin R8

R1950 22 5% 1/16W MF-LF 402 — LPC_AD<0>
R1951 22 5% 1/16W MF-LF 402 — LPC_AD<1>
R1952 22 5% 1/16W MF-LF 402 — LPC_AD<2>
R1953 22 5% 1/16W MF-LF 402 — LPC_AD<3>

R1961 10K 5% 1/16W MF-LF 402
Strap for Boot ROM Selection (See HDA_SDOUT)

GND65	U24	GND98	Y26
GND66	U26	GND99	Y27
GND67	U39	GND100	AB18
GND68	U4	GND101	H34
GND69	U8	GND102	AB20
GND70	V16	GND103	AB21
GND71	V17	GND104	AB23
GND72	V18	GND105	AB24
GND73	V20	GND106	AB25
GND74	V22	GND107	AB26
GND75	V24	GND108	AB27
GND76	V26	GND109	AB28
GND77	V27	GND110	AB34
GND78	V28	GND[redacted]	AB37
GND79	V33	GND[redacted]	AB4
GND80	V37	GND[redacted]	[redacted]
GND81	V4	GND[redacted]	[redacted]
GND82	V40	GND[redacted]	[redacted]
GND83	V7	GND[redacted]	[redacted]
GND84	W20	GND[redacted]	[redacted]
GND85	W22	GND118	AC5
GND86	W24	GND119	AD16
GND87	W36	GND120	AD17
GND88	W40	GND121	AD18
GND89	W43	GND122	AD19
GND90	Y16	GND123	AD20
GND91	Y17	GND124	AD24
GND92	Y18	GND125	AD25
GND93	Y19	GND126	AD26
GND94	Y20	GND127	AD27
GND95	Y22	GND128	AD28
GND96	Y24	GND129	AD33
GND97	Y25	GND130	AD34

=PP3V3_S0_MCP_GPIO

MCP_RS232_SOUT_L	R1989	8.2K	5% 1/16W MF-LF 402
PCI_REQ0_L	R1990	8.2K	5% 1/16W MF-LF 402
PCI_REQ1_L	R1991	8.2K	5% 1/16W MF-LF 402
CRTMUX_SEL_TV_L	R1992	8.2K	5% 1/16W MF-LF 402
MCP_RS232_SIN_L	R1994	8.2K	5% 1/16W MF-LF 402

MCP PCI & LPC

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 19 OF 98

OMIT

U1400
MCP79-TOPO-B
BGA
(8 OF 11)

SATA

90 38 OUT SATA_HDD_R2D_C_P — AJ7 SATA_A0_TX_P
90 38 OUT SATA_HDD_R2D_C_N — AJ6 SATA_A0_TX_N
90 38 IN SATA_HDD_D2R_N — AJ5 SATA_A0_RX_N
90 38 IN SATA_HDD_D2R_P — AJ4 SATA_A0_RX_P

90 38 OUT SATA_ODD_R2D_C_P — AJ11 SATA_A1_TX_P
90 38 OUT SATA_ODD_R2D_C_N — AJ10 SATA_A1_TX_N
90 38 IN SATA_ODD_D2R_N — AJ9 SATA_A1_RX_N
90 38 IN SATA_ODD_D2R_P — AK9 SATA_A1_RX_P

[redacted]

7 TP_SATA_C_D2RN — SATA_B0_RX_N
7 TP_SATA_C_D2RP — SATA_B0_RX_P

7 TP_SATA_D_R2D_CP — AM4 SATA_B1_TX_P
7 TP_SATA_D_R2D_CN — AL3 SATA_B1_TX_N
7 TP_SATA_D_D2RN — AL4 SATA_B1_RX_N
7 TP_SATA_D_D2RP — AK3 SATA_B1_RX_P

7 TP_SATA_E_R2D_CP — AN1 SATA_C0_TX_P
7 TP_SATA_E_R2D_CN — AM1 SATA_C0_TX_N
7 TP_SATA_E_D2RN — AM2 SATA_C0_RX_N
7 TP_SATA_E_D2RP — AM3 SATA_C0_RX_P

[redacted]

7 TP_MCP_SATALED_L — E12 SATA_LED#

23 PP1V05_S0_MCP_PLL_SATA — AE16 +V_PLL_SATA
84 mA (A01)

8 =PP1V05_S0_MCP_SATA_DVDD0
43 mA (A01, DVDD0 & 1)
Minimum 1.025V for Gen2 support
AF19 +DVDD0_SATA1
AG16 +DVDD0_SATA2
AG17 +DVDD0_SATA3
AG19 +DVDD0_SATA4

9 =PP1V05_S0_MCP_SATA_DVDD1
AH17 +DVDD1_SATA1
AH19 +DVDD1_SATA2

8 =PP1V05_S0_MCP_SATA_AVDD0
127 mA (A01, AVDD0 & 1)
Minimum 1.025V for Gen2 support
AJ12 +AVDD0_SATA1
AN11 +AVDD0_SATA2
AK12 +AVDD0_SATA3
AK13 +AVDD0_SATA4
AL12 +AVDD0_SATA5
AM11 +AVDD0_SATA6

[redacted]

AM14 +AVDD1_SATA4

90 MCP_SATA_TERMP — AE3 SATA_TERMP

R2010
2.49K
1%
1/16W
MF-LF
402

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

USB

External A
USB0_P C29 — USB_EXTA_P — B1 39 91
USB0_N D29 — USB_EXTA_N — B1 39 91

AirPort (PCIe Mini-Card)
USB1_P C28 — USB_MINI_P — B1 9 91
USB1_N D28 — USB_MINI_N — B1 9 91

External D
USB2_P A28 — USB_EXTD_P — B1 9 91
USB2_N B28 — USB_EXTD_N — B1 9 91

Camera
USB3_P F29 — USB_CAMERA_P — B1 30 91
USB3_N G29 — USB_CAMERA_N — B1 30 91

IR
USB4_P K27 — USB_IR_P — B1 40 91
USB4_N [redacted]

[redacted]

USB6_N [redacted] — USB_B1_N — B1 30 91

External B
USB7_P D27 — USB_EXTB_P — B1 39 91
USB7_N E27 — USB_EXTB_N — B1 39 91

ExpressCard
USB8_P K25 — USB_EXCARD_P — B1 31 91
USB8_N L25 — USB_EXCARD_N — B1 31 91

External C
USB9_P H25 — USB_EXTC_P — B1 91 96 98
USB9_N J25 — USB_EXTC_N — B1 91 96 98

USB10_P F25 — TP_USB_10P — 7
USB10_N G25 — TP_USB_10N

USB11_P K23 — TP_USB_11P — 7
USB11_N L23 — TP_USB_11N — 7

=PP3V3_S5_MCP_GPIO — 8 18

R2051
8.2K
5%
1/16W
MF-LF
402

R2053
8.2K
5%
1/16W
MF-LF
402

R2050
8.2K
5%
1/16W
MF-LF
402

R2052
8.2K
5%
1/16W
MF-LF
402

USB_OC0#/GPIO_25 L21 — USB_EXTA_OC_L — IN 39
USB_OC1#/GPIO_26 K21 — USB_EXTB_OC_L — IN 39
USB_OC2#/GPIO_27/MGPIO — USB_EXTC_OC_L — IN 98
USB_OC3#/GPIO_28/MGPIO — EXCARD_OC_L — IN 31 42

[redacted]

R2060
806
1%
1/16W
MF-LF
402

GND131 AD35
GND132 AD37
GND133 AD38
GND134 AE22
GND135 AE24
GND136 AE39
GND137 AE4
GND138 AD6
GND139 AF16
GND140 AF17
GND141 AF18
GND142 AF20
GND143 AF22
GND144 AF26
GND145 AF27
GND146 AF28
GND147 AF33
GND148 AF34
GND149 [redacted]
GND150 [redacted]

[redacted]

GND156 AG40
GND157 AH18
GND158 AH20
GND159 AH22
GND160 AH24

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP SATA & USB

SYNC_MASTER=T18_MLB — SYNC_DATE=06/06/2008

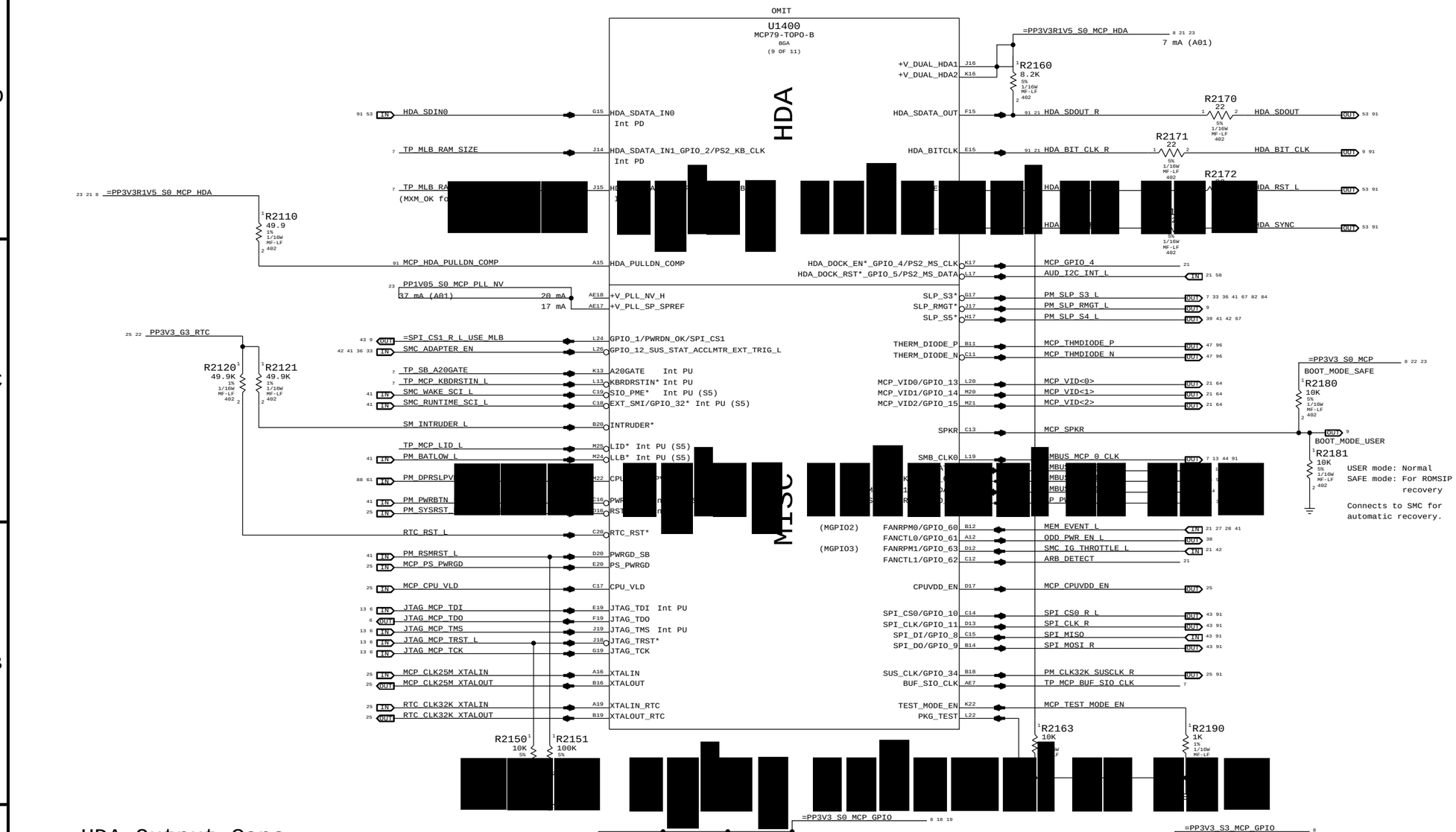
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

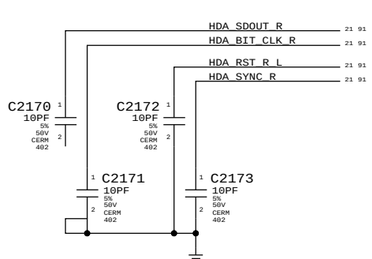
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 20 OF 98	



HDA Output Caps

For EMI Reduction on HDA interface



BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP HDA & MISC

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 21 OF 98

OMIT

U1400
MCP79-TOPO-B
BGA
(11 OF 11)

GND

AH26	GND161	GND253	AV40
AH33	GND162	GND254	BA1
AH34	GND163	GND255	BA4
AH37	GND164	GND256	AW31
AH38	GND165	GND257	AY6
AJ39	GND166	GND258	L35
AJ8	GND167	GND259	BC33
AK10	GND168	GND260	BC37
AK33	GND169	GND261	BC41
AK34	GND170	GND262	AY14
AK37	GND171	GND263	BC5
AK4	GND172	GND264	C2
AK40	GND173	GND265	D10
AL36	GND174	GND266	D14
AL40	GND175	GND267	D15
AL5	GND176	GND268	D18
AM10	GND177	GND269	D19
AM16	GND178	GND270	D22
AM18	GND179	GND271	D23
AM20	GND180	GND272	D26
AM22	GND181	GND273	D30
AM24	GND182	GND274	D37
AM26	GND183	GND275	D6
AM30	GND184	GND276	E13
AM34	GND185	GND277	E17
AM35	GND186	GND278	E21
AM37	GND187	GND279	E25
AM38	GND188	GND280	E29
AM5	GND189	GND281	E33
AM6	GND190	GND282	F12
AM7	GND191	GND283	F16
AM9	GND192	GND284	F32
AP26	GND193	GND285	F8
AN28	GND194	GND286	G10
AN30	GND195	GND287	G12
AN39	GND196	GND288	G14
AN4	GND197	GND289	G16
Y7	GND198	GND290	BC12
AP10	GND199	GND291	G22
AU26	GND200	GND292	G24
AP14	GND201	GND293	AW20
AU14	GND202	GND294	G34
AP28	GND203	GND295	G4
AP32	GND204	GND296	G43
AP34	GND205	GND297	G6
AP36	GND206	GND298	G8
AP37	GND207	GND299	H11
AP4	GND208	GND300	H15
AP40	GND209	GND301	AW35
AP7	GND210	GND302	H23
AW23	GND211	GND303	AN8
AR28	GND212	GND304	G40
AR32	GND213	GND305	J12
AR40	GND214	GND306	J8
AT10	GND215	GND307	K10
AR12	GND216	GND308	K12
AT13	GND217	GND309	K18
AT29	GND218	GND310	K26
AT33	GND219	GND311	K37
AT6	GND220	GND312	K4
AT7	GND221	GND313	K40
AT9	GND222	GND314	K8
AY21	GND223	GND315	AU1
AY22	GND224	GND316	L40
L12	GND225	GND317	L43
AU12	GND226	GND318	L5
AU28	GND227	GND319	M10
AP33	GND228	GND320	M34
AU32	GND229	GND321	M35
AR30	GND230	GND322	M37
AU36	GND231	GND323	Y28
AU38	GND232	GND324	Y33
AU4	GND233	GND325	Y34
G28	GND234	GND326	Y35
F20	GND235	GND327	Y37
AV28	GND236	GND328	Y38
AV32	GND237	GND329	AB17
AV36	GND238	GND330	AB16
AV4	GND239	GND331	AN26
AV7	GND240	GND332	AD7
AW11	GND241	GND333	M11
G20	GND242	GND334	AA4
AR43	GND243	GND335	AB19
AW43	GND244	GND336	AY13
AY10	GND245	GND337	P11
AV12	GND246	GND338	Y6
AY30	GND247	GND339	T11
AY33	GND248	GND340	V11
AY34	GND249	GND341	Y11
AY37	GND250	GND342	AH16
AY38	GND251	GND343	T22
AY41	GND252		

OMIT

U1400
MCP79-TOPO-B
BGA
(10 OF 11)

POWER

45 23 8 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

=PP1V05_S0_MCP_FSB 8 9 14 23
1139 mA 1182 mA (A01)

AK25	+VDD_CORE1	+VTT_CPU1	R32
AC23	+VDD_CORE2	+VTT_CPU2	AC32
U25	+VDD_CORE3	+VTT_CPU3	E40
AH12	+VDD_CORE4	+VTT_CPU4	J36
AG10	+VDD_CORE5	+VTT_CPU5	N32
AG5	+VDD_CORE6	+VTT_CPU6	T32
Y21	+VDD_CORE7	+VTT_CPU7	U32
Y23	+VDD_CORE8	+VTT_CPU8	V32
AA16	+VDD_CORE9	+VTT_CPU9	W32
AA26	+VDD_CORE10	+VTT_CPU10	P31
AA27	+VDD_CORE11	+VTT_CPU11	AF32
AA28	+VDD_CORE12	+VTT_CPU12	AE32
AC16	+VDD_CORE13	+VTT_CPU13	AH32
AC17	+VDD_C[redacted]	+VTT_CPU14	AJ32
[redacted]	[redacted]	[redacted]	[redacted]
AC22	+VDD_CORE20	+VTT_CPU20	B41
AC25	+VDD_CORE21	+VTT_CPU21	B42
AC26	+VDD_CORE22	+VTT_CPU22	C40
AC27	+VDD_CORE23	+VTT_CPU23	C41
AC28	+VDD_CORE24	+VTT_CPU24	C42
AD21	+VDD_CORE25	+VTT_CPU25	D39
AD23	+VDD_CORE26	+VTT_CPU26	D40
W27	+VDD_CORE27	+VTT_CPU27	D41
V25	+VDD_CORE28	+VTT_CPU28	E38
AA18	+VDD_CORE29	+VTT_CPU29	E39
AE19	+VDD_CORE30	+VTT_CPU30	F37
AE21	+VDD_CORE31	+VTT_CPU31	F38
AE23	+VDD_CORE32	+VTT_CPU32	F39
AE25	+VDD_CORE33	+VTT_CPU33	G36
AE26	+VDD_CORE34	+VTT_CPU34	G37
AE27	+VDD_CORE35	+VTT_CPU35	G38
AE28	+VDD_CORE36	+VTT_CPU36	H35
AF10	+VDD_CORE37	+VTT_CPU37	H37
AF11	+VDD_CORE38	+VTT_CPU38	J34
AA19	+VDD_CORE39	+VTT_CPU39	J35
AF2	+VDD_CO[redacted]	+VTT_CPU40	K33
AF21	+VDD_CO[redacted]	+VTT_CPU41	K34
[redacted]	[redacted]	[redacted]	[redacted]
AH23	+VDD_CORE47	+VTT_CPU47	M32
AF9	+VDD_CORE48	+VTT_CPU48	M33
AA20	+VDD_CORE49	+VTT_CPU49	N31
AG11	+VDD_CORE50	+VTT_CPU50	P32
AG12	+VDD_CORE51	+VTT_CPU51	Y32
AG21	+VDD_CORE52	+VTT_CPU52	AA32
AG23	+VDD_CORE53		
AG25	+VDD_CORE54	+VTT_CPUCLK	AG32
AG3	+VDD_CORE55		
AG4	+VDD_CORE56		
AA21	+VDD_CORE57		
AG6	+VDD_CORE58	+3.3V_1	AD10
AG7	+VDD_CORE59	+3.3V_2	AE8
AG8	+VDD_CORE60	+3.3V_3	AB10
AG9	+VDD_CORE61	+3.3V_4	AD9
AH1	+VDD_CORE62	+3.3V_5	Y10
AH10	+VDD_CORE63	+3.3V_6	AB11
AH11	+VDD_CORE64	+3.3V_7	AA8
W26	+VDD_CORE65	+3.3V_8	Y9
AH2	+VDD_CORE66		
AA23	+VDD_CORE[redacted]		
W28	+VDD_CORE[redacted]		
[redacted]	[redacted]	[redacted]	[redacted]
AH6	+VDD_CORE74		
AH7	+VDD_CORE75	+3.3V_DUAL_USB1	G26
AH9	+VDD_CORE76	+3.3V_DUAL_USB2	H27
AA24	+VDD_CORE77	+3.3V_DUAL_USB3	J28
W21	+VDD_CORE78	+3.3V_DUAL_USB4	K28
W23	+VDD_CORE79		
W25	+VDD_CORE80		
AF12	+VDD_CORE81		
		+VDD_AUXC1	T21
		+VDD_AUXC2	U21
A20	+VBAT	+VDD_AUXC3	V21

43 mA

=PP3V3_S0_MCP 8 21 23
450 mA (A01)

250 mA

=PP1V05_S5_MCP_VDD_AUXC 8 23
105 mA (A01)

25 21 PP3V3_G3_RTC
10 uA (G3)
80 uA (S0)

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Power & Ground

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 22 OF 98	

MCP Core Power
=PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)

C2500 4.7UF 20% 4V X5R 402
C2501 4.7UF 20% 4V X5R 402
C2502 4.7UF 20% 4V X5R 402
C2503 4.7UF 20% 4V X5R 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

MCP PCIE (DVDD) Power
=PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)

C2515 4.7UF 20% 4V X5R 402
C2516 1UF 10% 10V X5R 402-1
C2517 1UF 10% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

MCP SATA (DVDD) Power
=PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)

C2520 4.7UF 20% 4V X5R 402
C2521 0.1UF 20% 10V CERM 402

[redacted]

131 mA (A01)

C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

=PP1V05_S0_MCP_AVDD_UF
333 mA (A01)

L2570 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)

C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF

PP1V05_S0_MCP_PEX_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
206 mA (A01)

MCP 1.05V AUX Power
=PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)

C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402

[redacted]

L575 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
127 mA (A01)

MCP FSB (VTT) Power
=PP1V05_S0_MCP_FSB
1182 mA (A01)

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

=PP1V05_S0_MCP_PLL_PEX_UF

L2582 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_PEX
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

C2582 4.7UF 20% 4V X5R 402
C2583 2.2UF 20% 6.3V CERM 402-LF

MCP Memory Power
=PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)

C2540 4.7UF 20% 4V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402

[redacted]

562 mA

C2580 4.7UF 20% 4V X5R 402
C2581 2.2UF 20% 16V X5R 603

PP1V05_S0_MCP_PLL_FSB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
270 mA (A01)

MCP 3.3V Power
=PP3V3_S0_MCP
450 mA (A01)

NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)

C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

=PP3V3_S0_MCP_PLL_UF
19 mA (A01)

L2555 30-OHM-1.7A 0402

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

PP3V3_S0_MCP_PLL_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
19 mA (A01)

C2555 2.2UF 20% 6.3V CERM 402-LF

L2584 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_SATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

C2584 4.7UF 20% 4V X5R 402
C2585 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V AUX/USB Power
=PP3V3_S5_MCP
266 mA (A01)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power
=PP3V3_ENET_MCP_RMGT
83 mA (A01)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2564 2.2UF 20% 6.3V CERM

[redacted]

L2586 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
87 mA (A01)

C2586 4.7UF 20% 4V X5R 402
C2587 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V/1.5V HDA Power
=PP3V3R1V5_S0_MCP_HDA
7 mA (A01)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2562 2.2UF 20% 6.3V CERM 402-LF

L2588 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_NV
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
37 mA (A01)

C2588 4.7UF 20% 4V X5R 402
C2589 2.2UF 20% 6.3V CERM 402-LF
C2590 0.1UF 20% 10V CERM 402

MCP79 Ethernet VRef

=PP3V3_ENET_MCP_RMGT

R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402

MCP_MII_VREF OUT

C2591 0.1UF 20% 10V CERM 402

=PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)

L2595 30-OHM-1.7A 0402

PP1V05_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
5 mA (A01)

C2595 4.7UF 20% 4V X5R 402
C2596 2.2UF 20% 6.3V CERM 402-LF

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Standard Decoupling

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 23 OF 98	

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

18 8 =PP3V3R1V8_S0_MCP_IFP_VDD
190 mA (A01, 1.8V)

C2610
2.2UF
20%
6.3V
CERM
402-LF

NO STUFF
L2650
30-OHM-1.7A
0402

NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

8 =PP3V3_S0_MCP_DAC_UF
206 mA (A01)

PP3V3_S0_MCP_DAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
206 mA (A01)

NO STUFF
C2650
2.2UF
20%
6.3V
CERM
402-LF

R2651
0
5%
1/10W
MF-LF
402

18 8 =PP1V05_S0_MCP_HDMI_VDD
95 mA (A01)

C2615
4.7UF
20%
4V
X5R
402

2.2UF
20%
6.3V
CERM
402-LF

90 18 MCP_HDMI_RSET
90 18 MCP_HDMI_VPROBE

NO STUFF
C2620
0.1UF
20%
10V
CERM
402

R2620
1K
1%
1/16W
MF-LF
402

90 18 MCP_IFPAB_RSET
90 18 MCP_IFPAB_VPROBE

NO STUFF
C2630
0.1UF
20%
10V
CERM
402

NO STUFF
R2630
1K
1%
1/16W
MF-LF
402

8 =PP3V3_S0_MCP_VPLL_UF
16 mA (A01)

0402

MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

C2640
4.7UF
20%
6.3V
CERM
603

C2641
2.2UF
20%
6.3V
CERM
402-LF

18 TP_MCP_RGB_RED — NC_MCP_RGB_RED
18 TP_MCP_RGB_GREEN — NC_MCP_RGB_GREEN
18 TP_MCP_RGB_BLUE — NC_MCP_RGB_BLUE
18 TP_MCP_RGB_HSYNC — NC_MCP_RGB_HSYNC
18 TP_MCP_RGB_VSYNC — NC_MCP_RGB_VSYNC
MAKE_BASE=TRUE NO_TEST=TRUE

90 18 CRT_IG_R_C_PR — NC_CRT_IG_R_C_PR
90 18 CRT_IG_G_Y_Y — NC_CRT_IG_G_Y_Y
90 18 CRT_IG_B_COMP_PB — NC_CRT_IG_B_COMP_PB
90 18 CRT_IG_HSYNC — NC_CRT_IG_HSYNC
90 18 CRT_IG_VSYNC — NC_CRT_IG_VSYNC
MAKE_BASE=TRUE NO_TEST=TRUE

18 [redacted] — NC_MCP_RGB_DAC_RSET
18 [redacted] — NC_MCP_RGB_DAC_VREF
90 18 [redacted] — NC_MCP_TV_DAC_RSET
90 18 MCP_TV_DAC_VREF — NC_MCP_TV_DAC_VREF
MAKE_BASE=TRUE NO_TEST=TRUE

18 MCP_CLK27M_XTALIN — NC_MCP_CLK27M_XTALIN
18 MCP_CLK27M_XTALOUT — NC_MCP_CLK27M_XTALOUT
MAKE_BASE=TRUE NO_TEST=TRUE

HDCP ROM

WF: Open question on which packge option(s) nVidia can support.

8 =PP3V3_S0_HDCPROM

C2690
0.1UF
20%
10V
CERM
402

NO STUFF

NO STUFF

U2695
AT24C08
SOIC

A0 1
A1 2
A2 3
GND 4
VCC 8
SDA 5 — =I2C_HDCPROM_SDA — B1 44
SCL 6 — =I2C_HDCPROM_SCL — A1 44
WP 7 — HDCPROM_WP

MCP Graphics Support

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

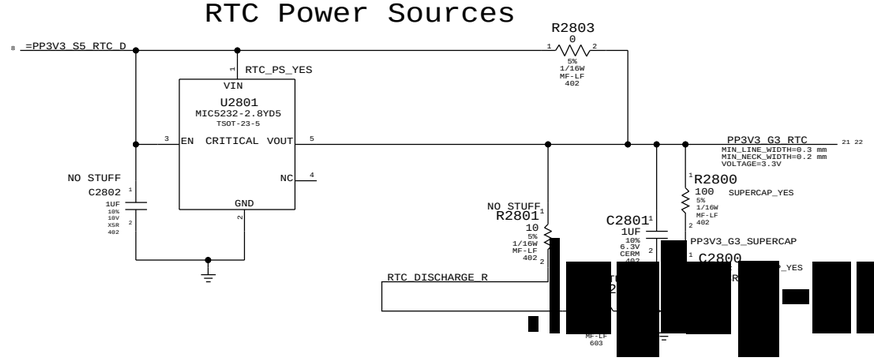
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE	SHT	OF
NONE	24	98

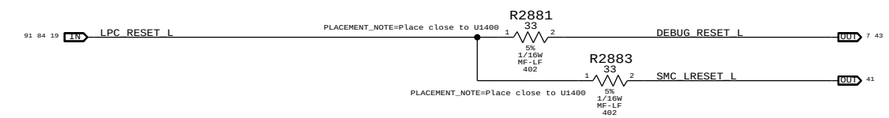
Current numbers from email Xiaowei Lin provided 11/12/2007 3:22pm (no official document number).

RTC Power Sources

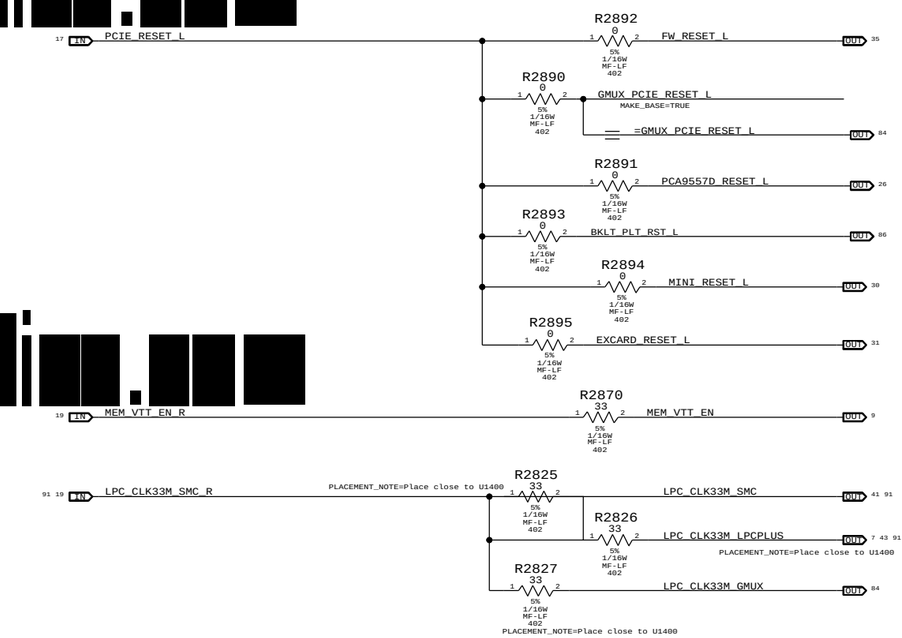


Platform Reset Connections

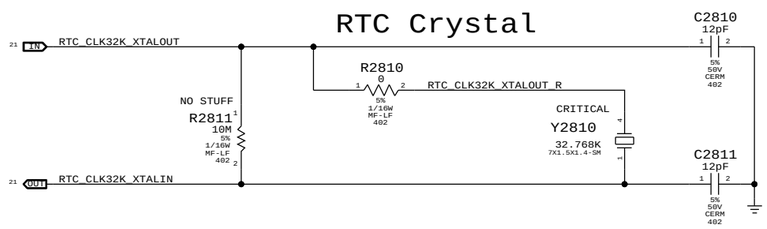
LPC Reset (Unbuffered)



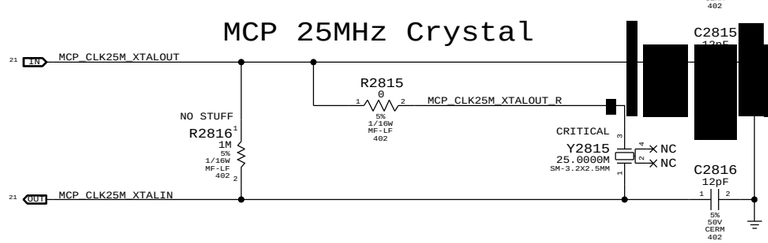
PCIE Reset (Unbuffered)



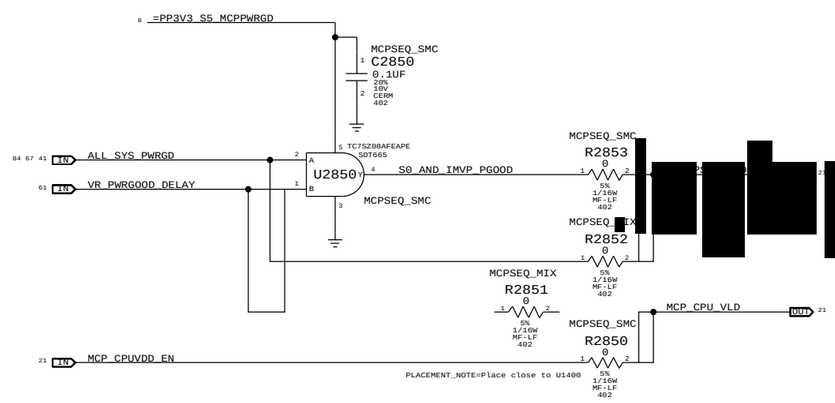
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



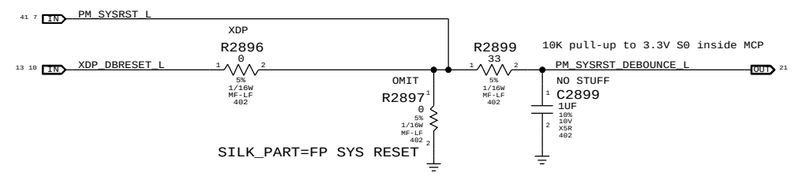
MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

Reset Button



SB Misc	
SYNC_MASTER=M98_MLB	SYNC_DATE=05/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 25	OF 98

Page Notes

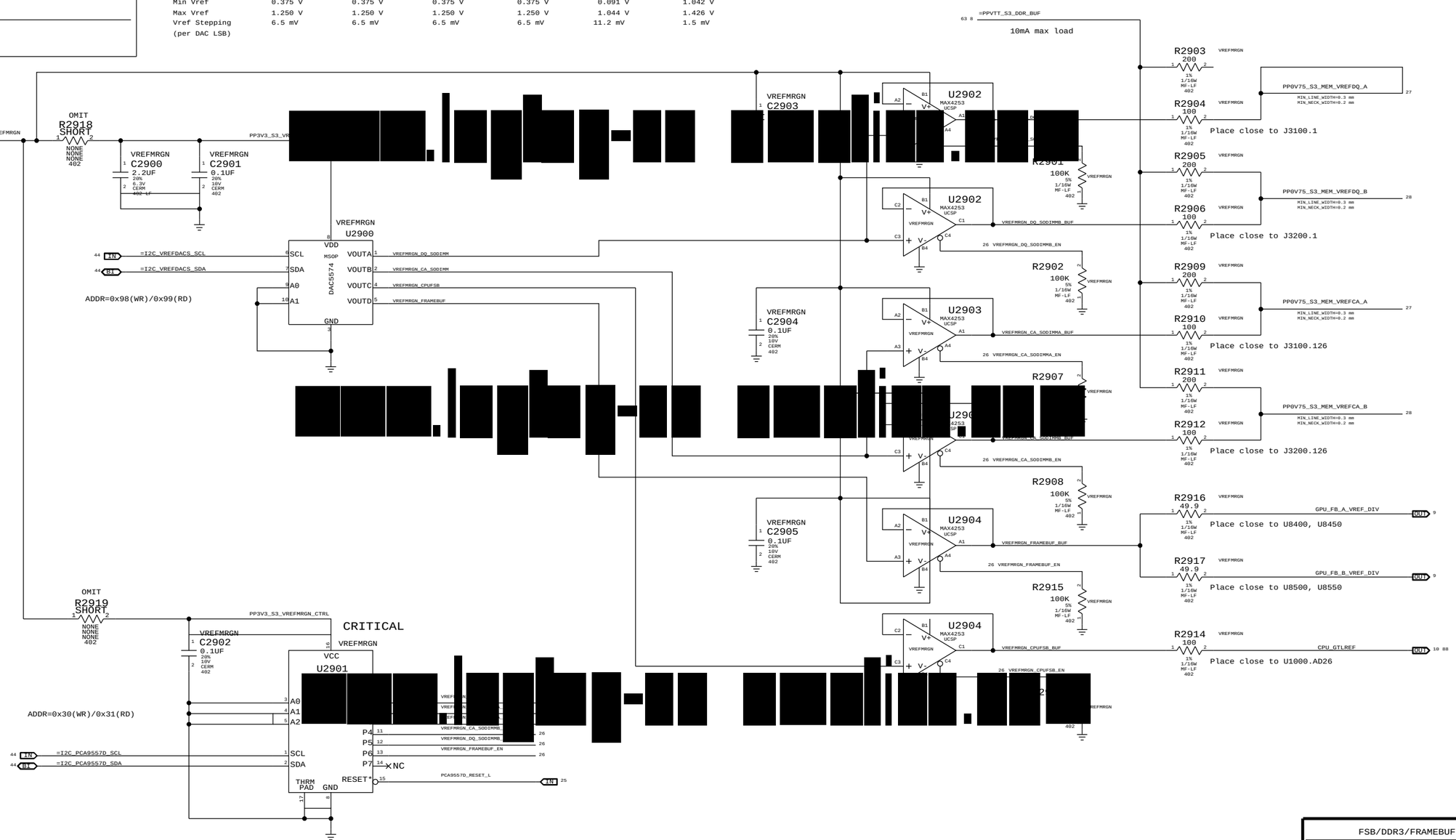
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel	MEM A VREF DQ A	MEM A VREF CA B	MEM B VREF DQ A	MEM B VREF CA B	CPU FSB VREF C	FRAME BUFFER VREF D
Min DAC code	0x00	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55	0xFF
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA	-59.04 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA	51.15 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V	1.248 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V	1.042 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V	1.426 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV	1.5 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3/FRAMEBUF Vref Margining

SYNC_MASTER=BEN_K20 SYNC_DATE=10/15/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 26 OF 98

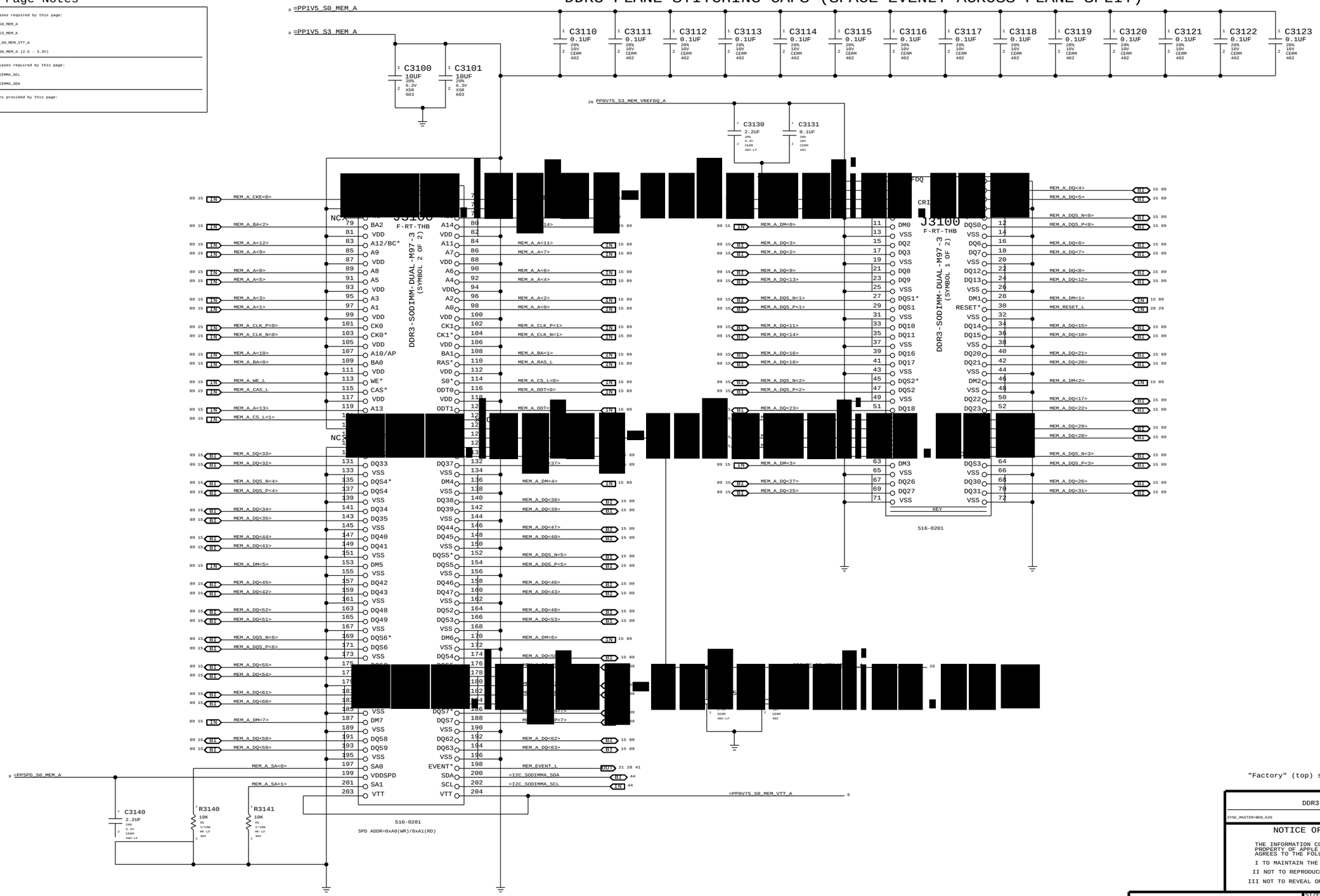
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)



"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=BEN_K20 SYNC_DATE=06/10/2009

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 27 OF 98	

Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

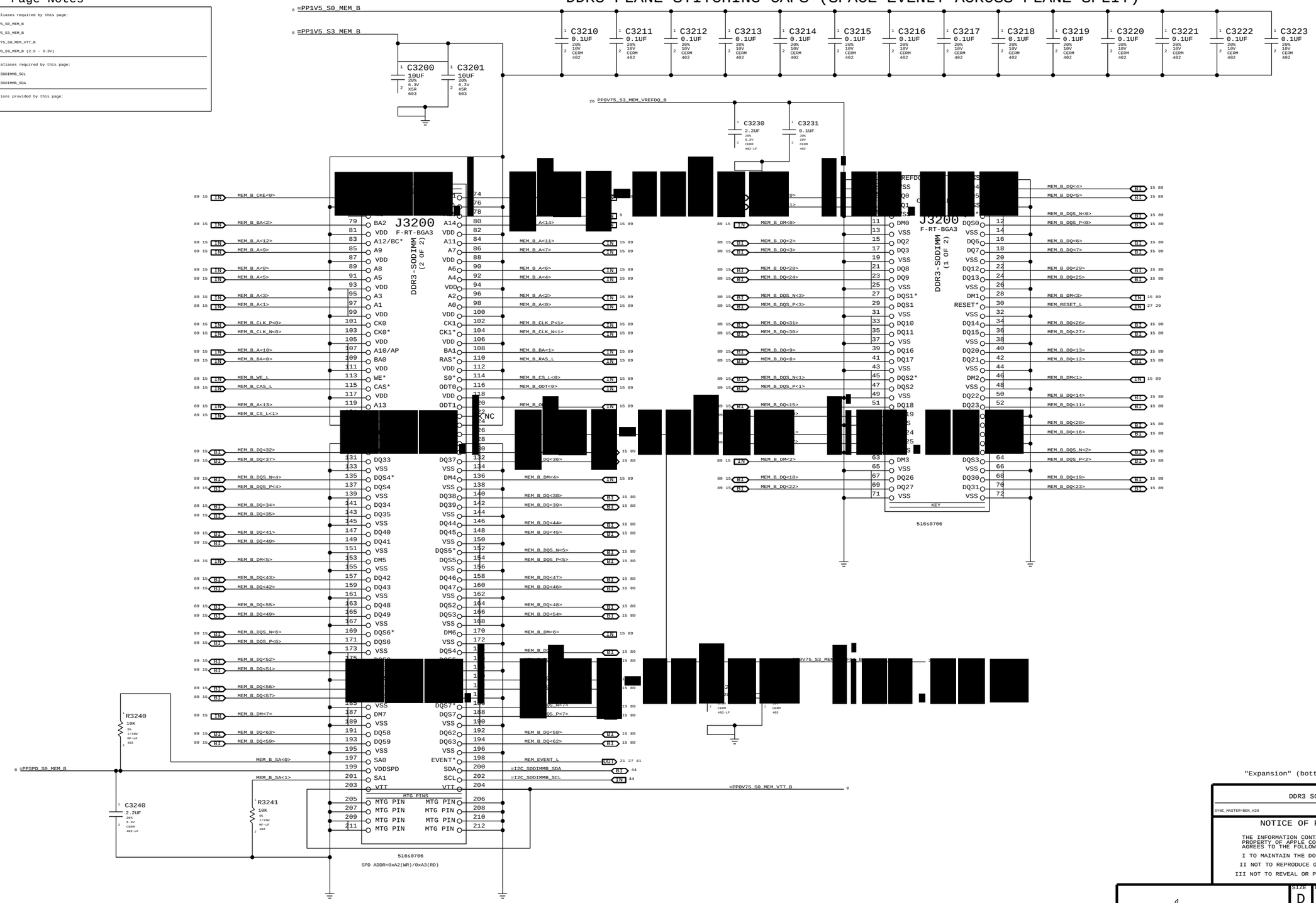
Signal aliases required by this page:

- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:

(NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)



"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

SYNC_MASTER=BEN_K20 SYNC_DATE=07/14/2009

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

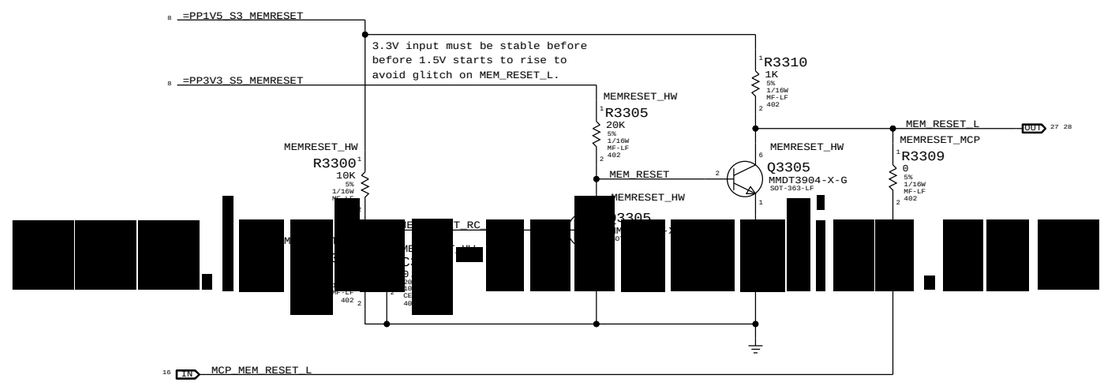
SIZE	DRAWING NUMBER	REV.
D	051-8071	B

SCALE	SHT	OF
NONE	28	98

www.laptop-schematics.com

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



www.laptop-schematics.com

DDR3 Support

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

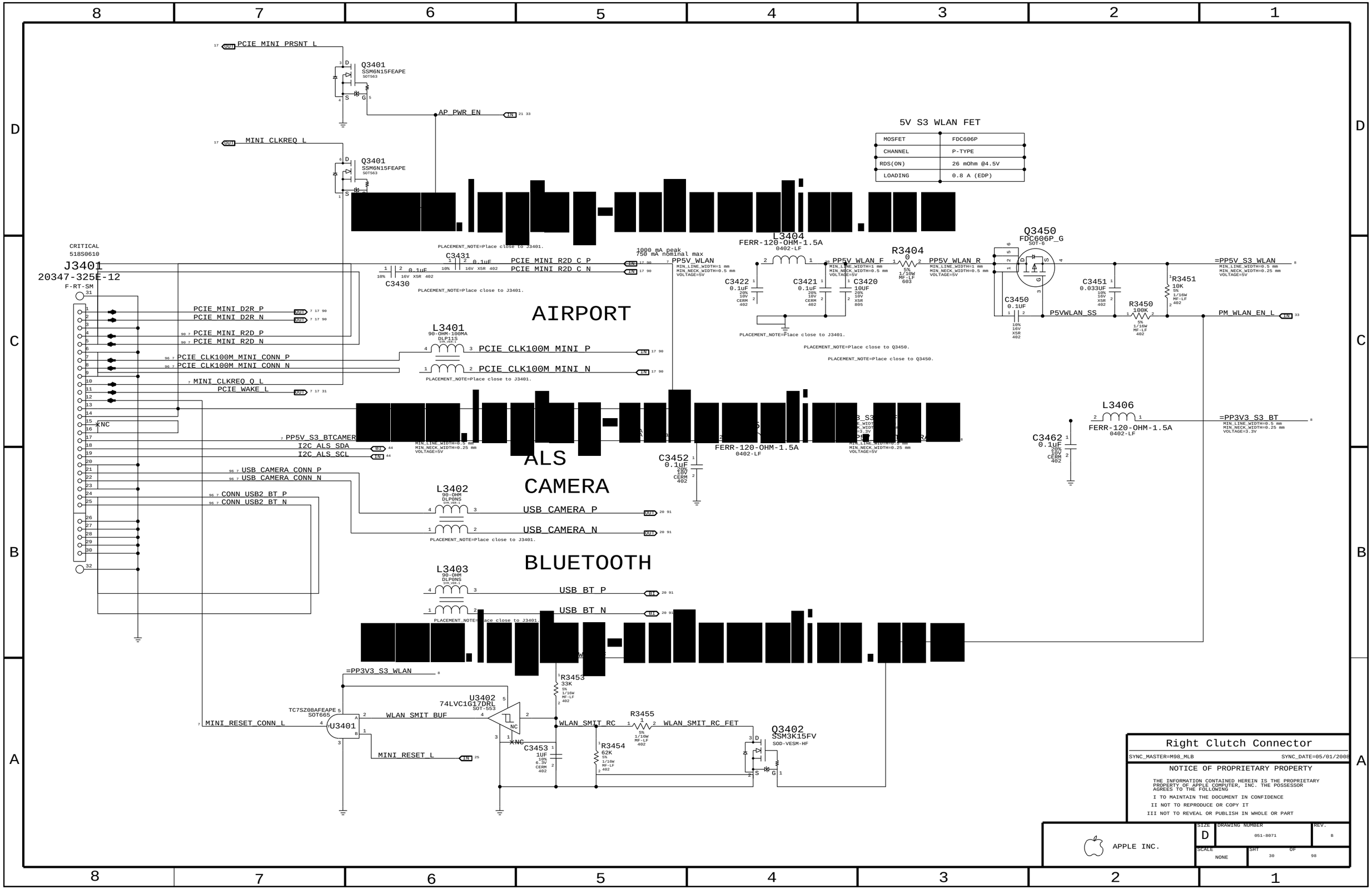
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 29 OF 98	


PCIE MINI PRSNT L
Q3401
SSM6N15FEAPE
SOT563
AP PWR EN
MINI CLKREQ L
Q3401
SSM6N15FEAPE
SOT563
5V S3 WLAN FET
MOSFET FDC606P
CHANNEL P-TYPE
RDS(ON) 26 mOhm @4.5V
LOADING 0.8 A (EDP)
CRITICAL
518S0610
J3401
20347-325E-12
F-RT-SM
PCIE MINI R2D C P
PCIE MINI R2D C N
PP5V_WLAN
C3431
0.1uF
C3430
0.1uF
PLACEMENT_NOTE=Place close to J3401.
1000 mA peak
750 mA nominal max
L3404
FERR-120-OHM-1.5A
0402-LF
PP5V_WLAN_F
PP5V_WLAN_R
R3404
0
C3422
0.1uF
C3421
0.1uF
C3420
10UF
Q3450
FDC606P_G
SOT-6
C3450
0.1UF
C3451
0.033UF
R3451
10K
R3450
100K
P5VWLAN_SS
=PP5V_S3_WLAN
PM_WLAN_EN_L
PCIE MINI D2R P
PCIE MINI D2R N
PCIE MINI R2D P
PCIE MINI R2D N
PCIE CLK100M MINI CONN P
PCIE CLK100M MINI CONN N
MINI CLKREQ_O_L
PCIE_WAKE_L
NC
L3401
90-OHM-100MA
DLP11S
PCIE CLK100M MINI P
PCIE CLK100M MINI N
AIRPORT
PP5V_S3_BTCAMERA
I2C_ALS_SDA
I2C_ALS_SCL
USB CAMERA CONN P
USB CAMERA CONN N
CONN USB2 BT P
CONN USB2 BT N
L3402
90-OHM
DLP0NS
USB_CAMERA_P
USB_CAMERA_N
ALS
CAMERA
C3452
0.1uF
FERR-120-OHM-1.5A
0402-LF
L3406
FERR-120-OHM-1.5A
0402-LF
=PP3V3_S3_BT
C3462
0.1uF
L3403
90-OHM
DLP0NS
USB_BT_P
USB_BT_N
BLUETOOTH
=PP3V3_S3_WLAN
R3453
33K
U3402
74LVC1G17DRL
SOT-553
TC7SZ08AFEAPE
SOT665
U3401
MINI_RESET_CONN_L
WLAN_SMIT_BUF
MINI_RESET_L
XNC
C3453
1UF
WLAN_SMIT_RC
R3455
1
WLAN_SMIT_RC_FET
R3454
62K
Q3402
SSM3K15FV
SOD-VESM-HF
Right Clutch Connector
SYNC_MASTER=M98_MLB
SYNC_DATE=05/01/2008
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE INC.
SIZE D
DRAWING NUMBER 051-8071
REV. 8
SCALE NONE
SHT 30 OF 98

EXPRESSCARD/34 FLEX CONNECTOR

ExpressCard Connector

SYNC_MASTER=BEN_K20 SYNC_DATE=10/15/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

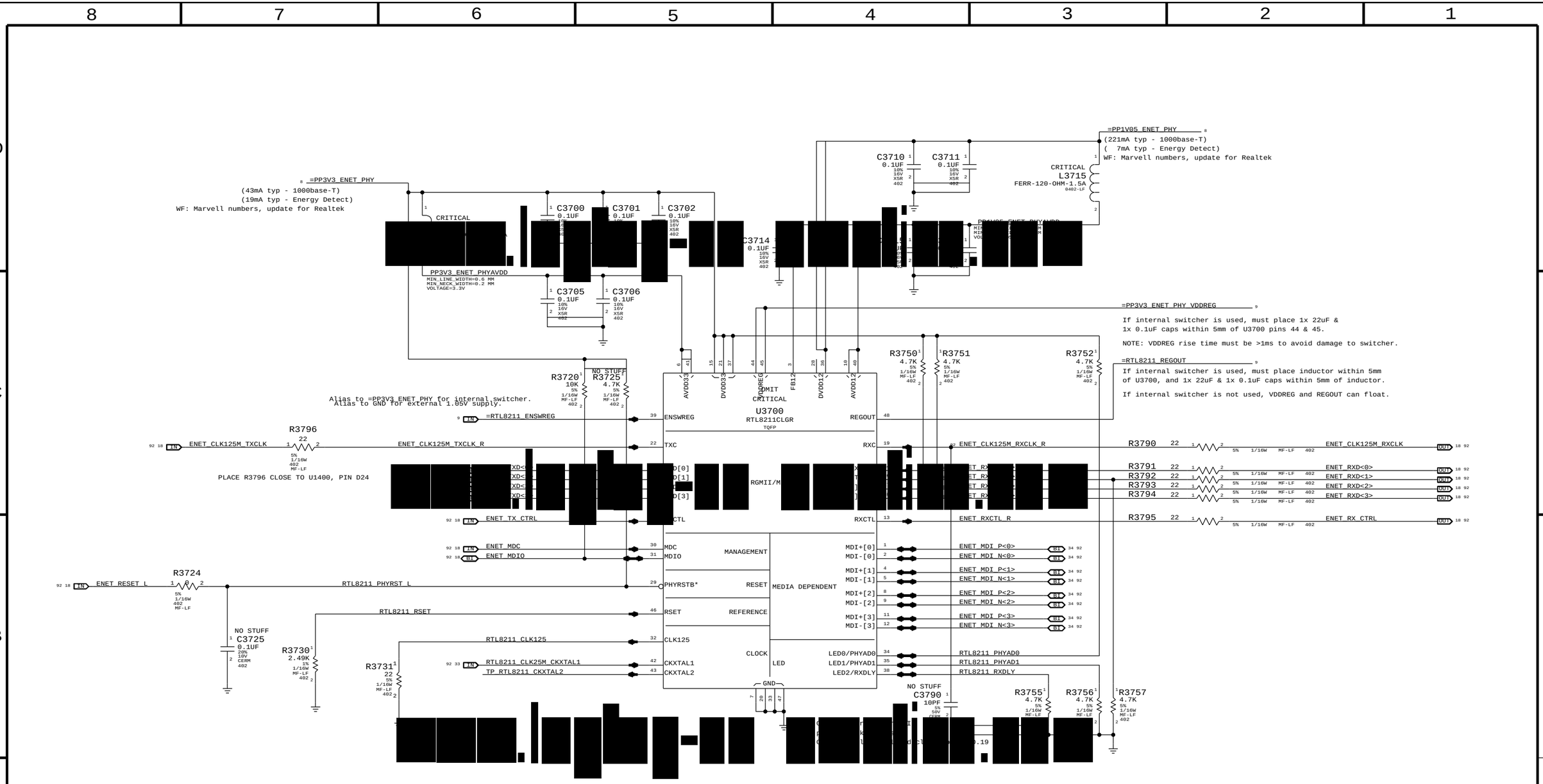
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 31 OF 98	



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/22/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

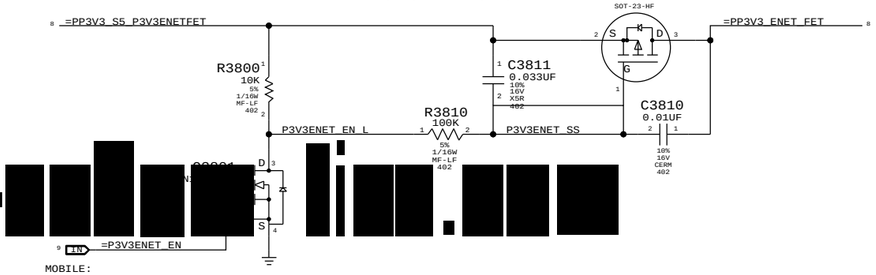
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 32 OF 98	

3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

CRITICAL



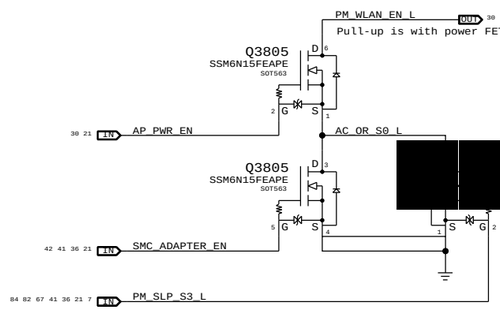
MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

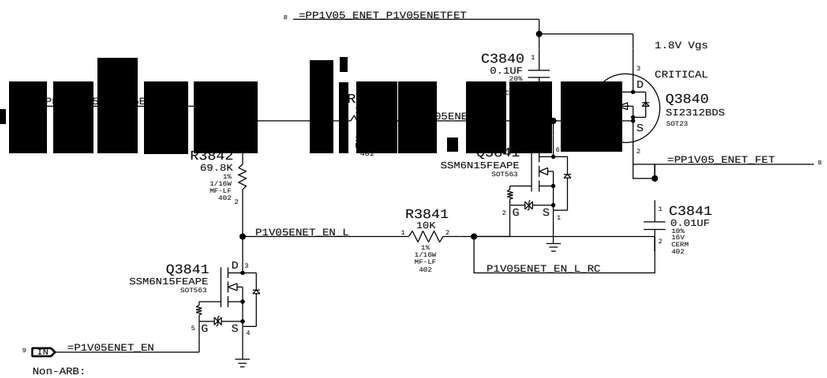
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



1.05V ENET FET



Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

PLACEMENT_NOTE=Place close to U1400

Ethernet & AirPort Support

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/15/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

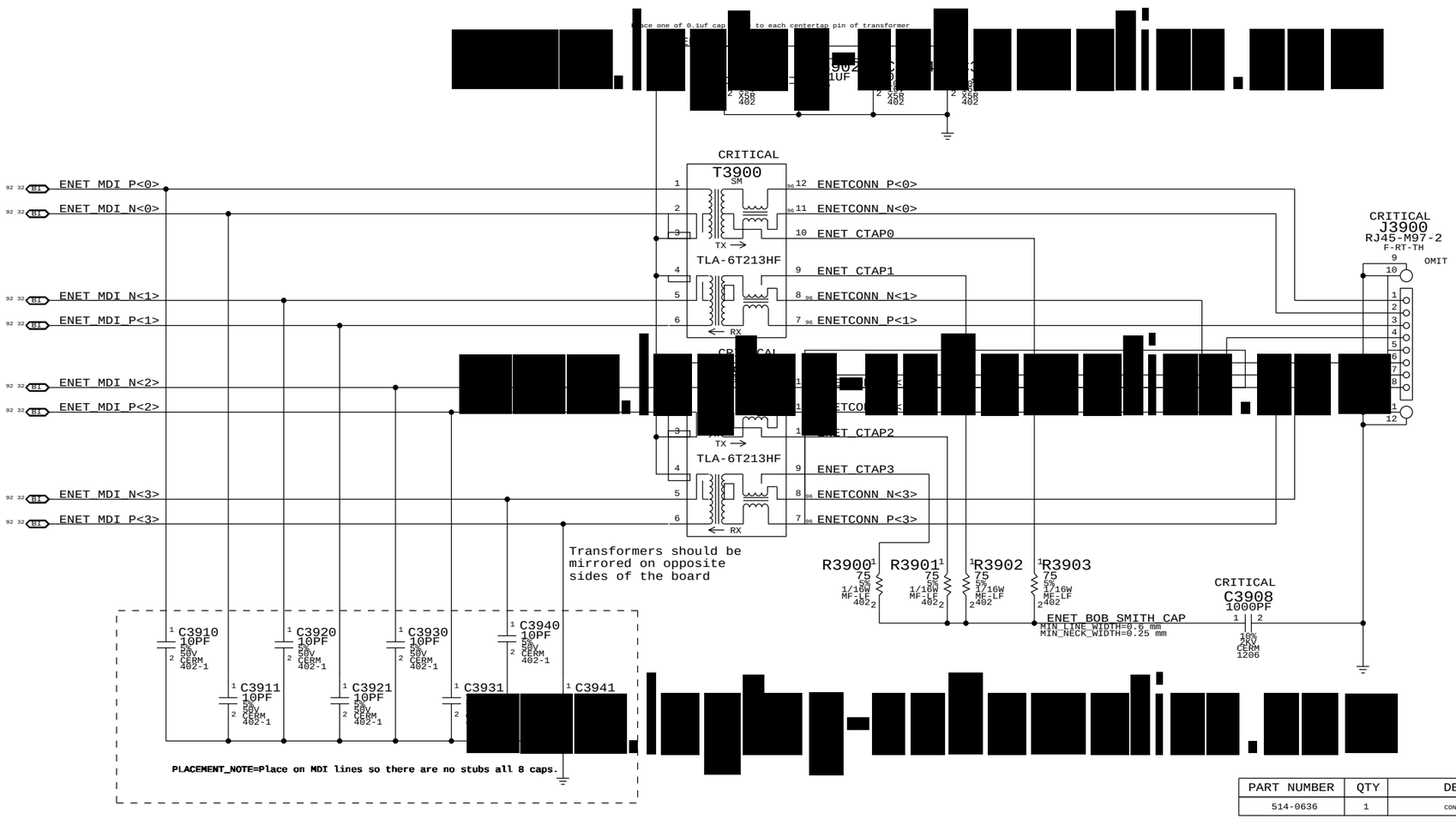
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 33 OF 98	

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0636	1	CONN,RJ45,HB,10/100TX	J3900	CRITICAL	

Ethernet Connector

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/15/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

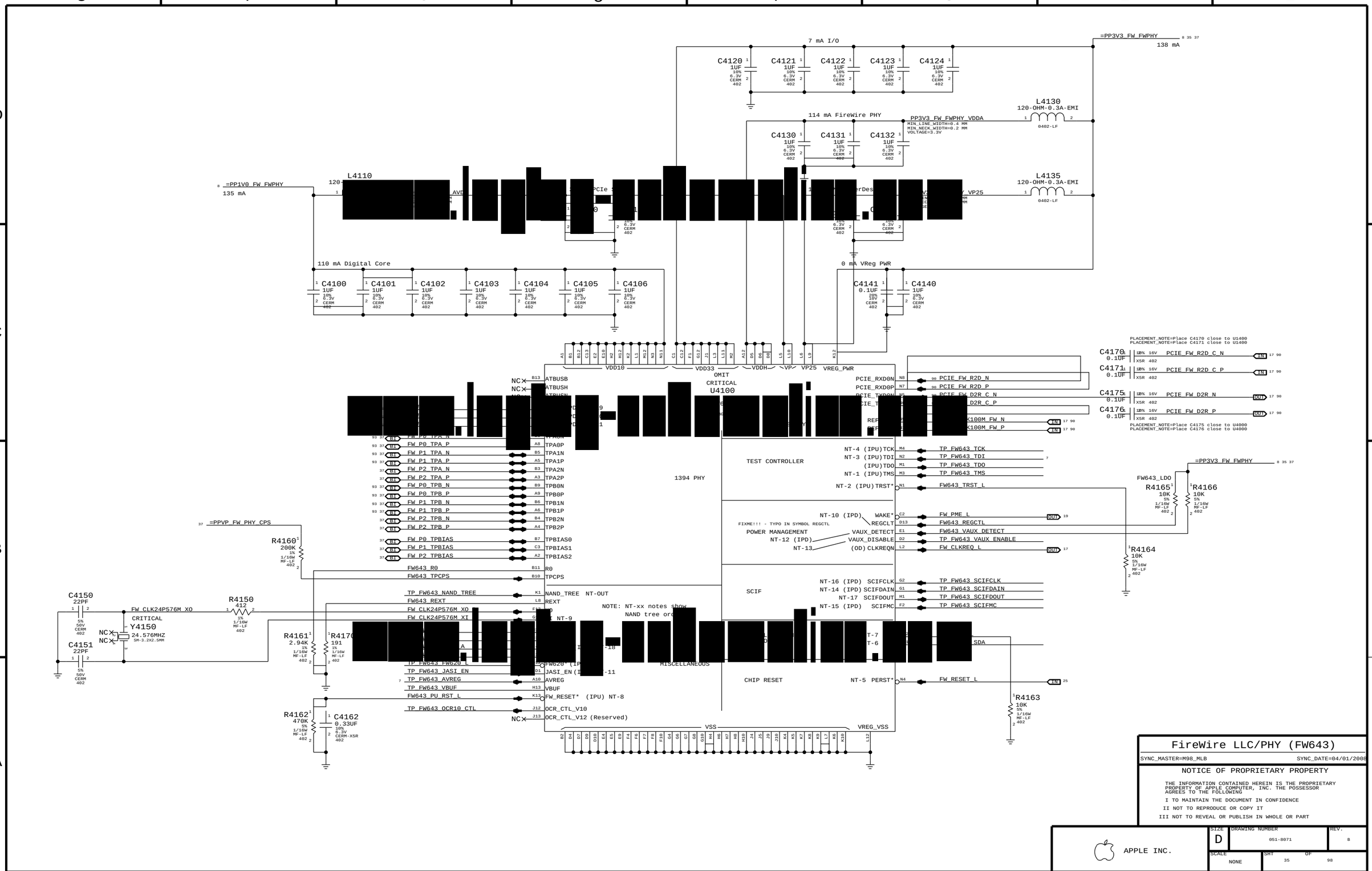
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 34 OF 98



FireWire LLC/PHY (FW643)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 35 OF 98

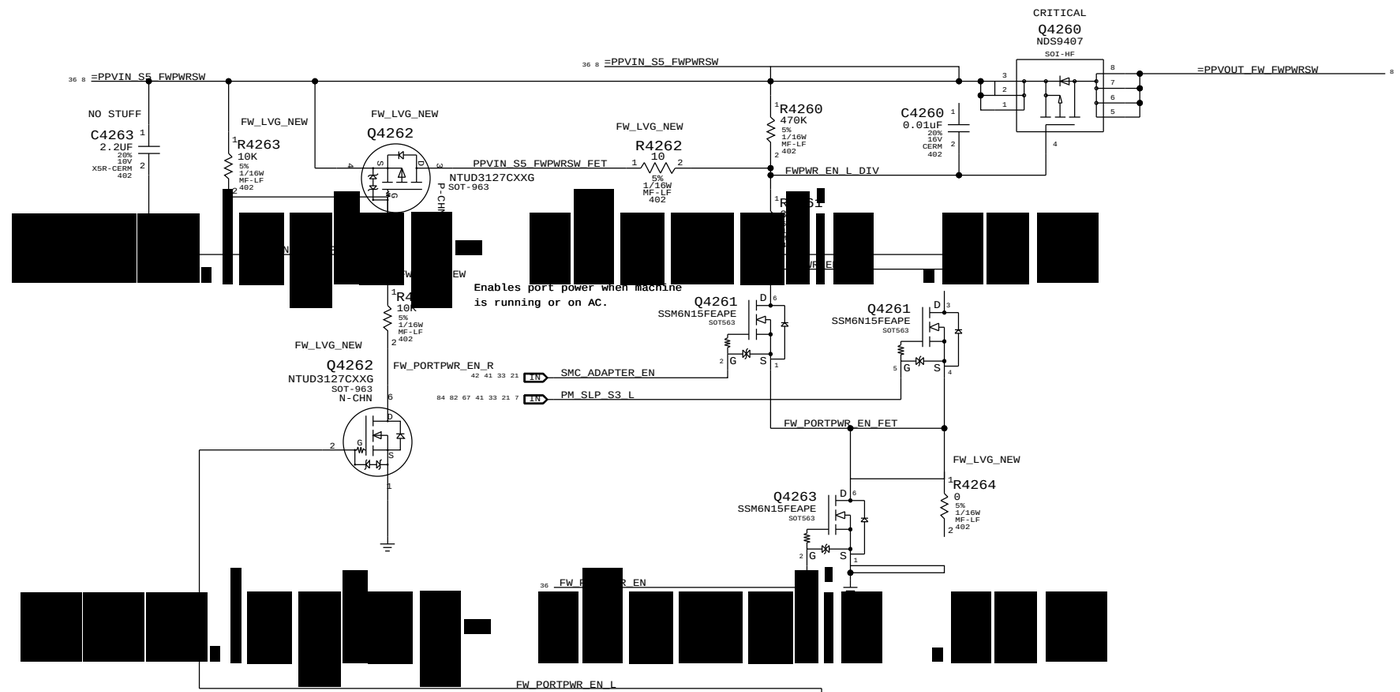
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

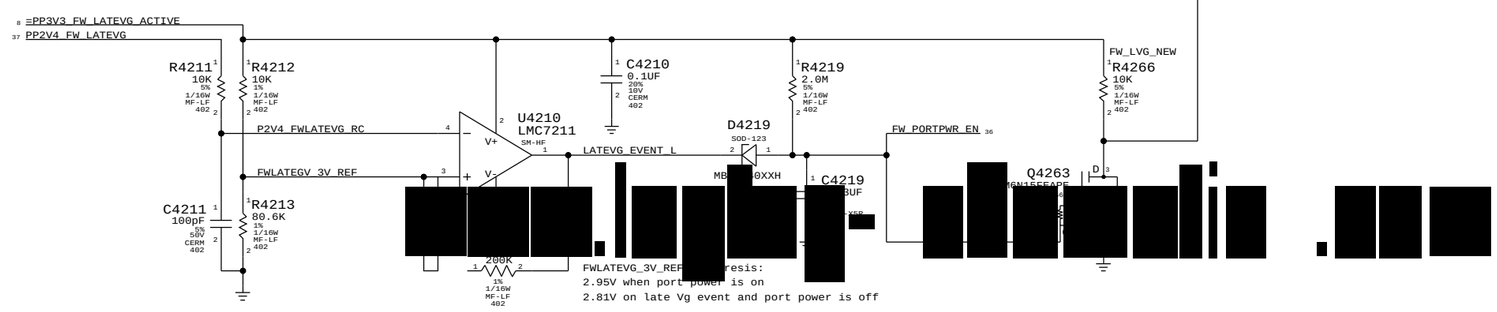
Signal aliases required by this page:
(NONE)

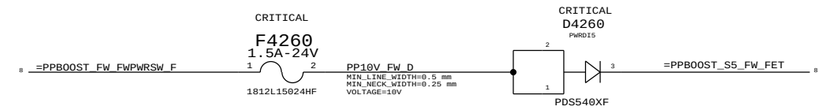
BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Late-VG Event Detection





FireWire Port Power

SYNC_MASTER=YWU_K20 SYNC_DATE=05/28/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 36 OF 98	

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

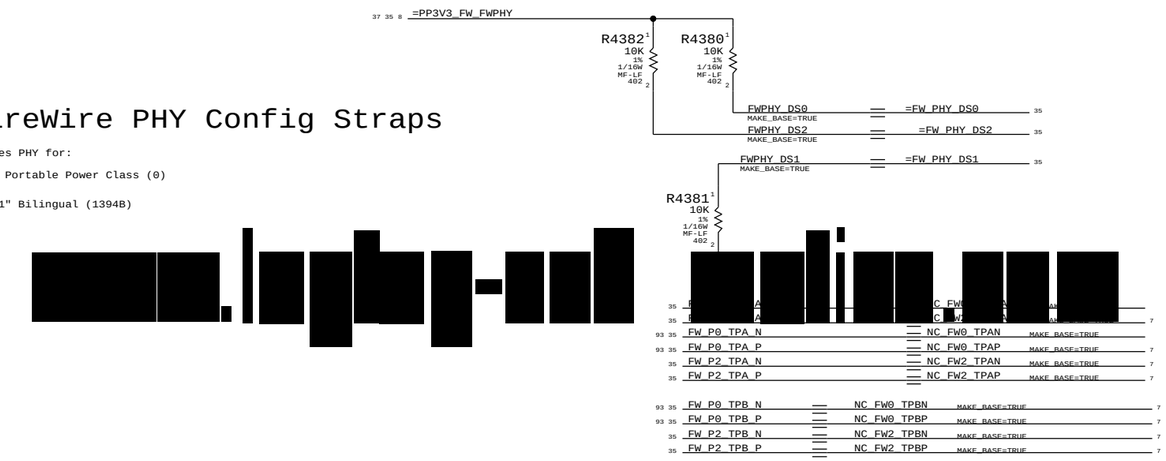
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

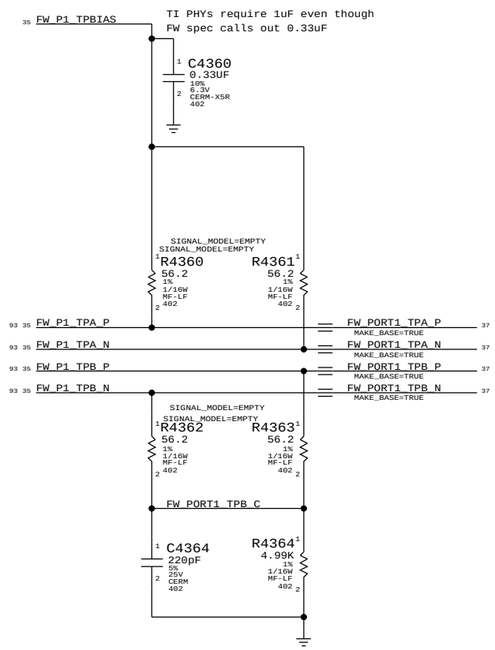
- 1-port Portable Power Class (0)

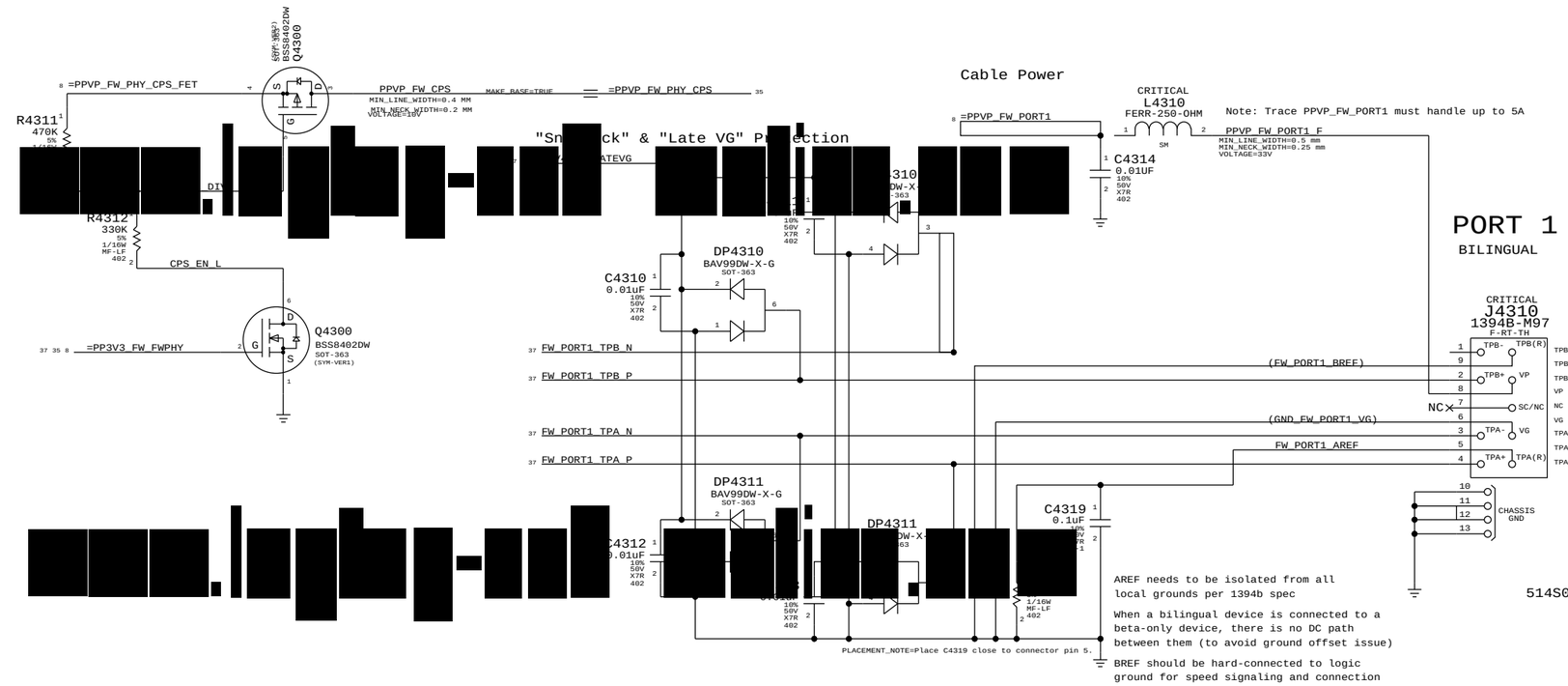
- Port "1" Bilingual (1394B)



Termination

Place close to FireWire PHY



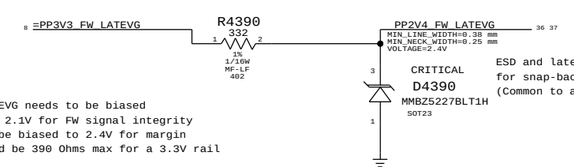


AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

Late-VG Protection Power



ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

FireWire Ports

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

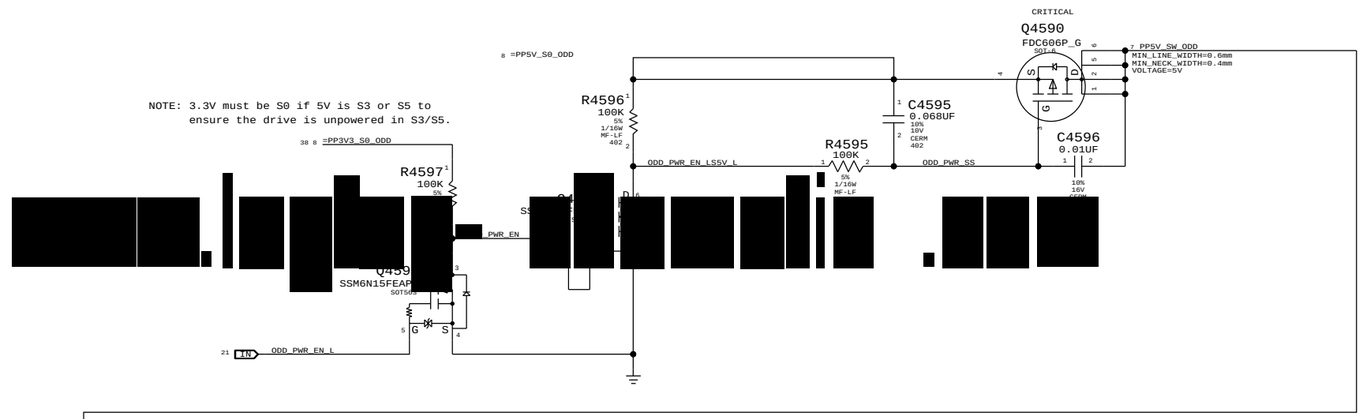
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

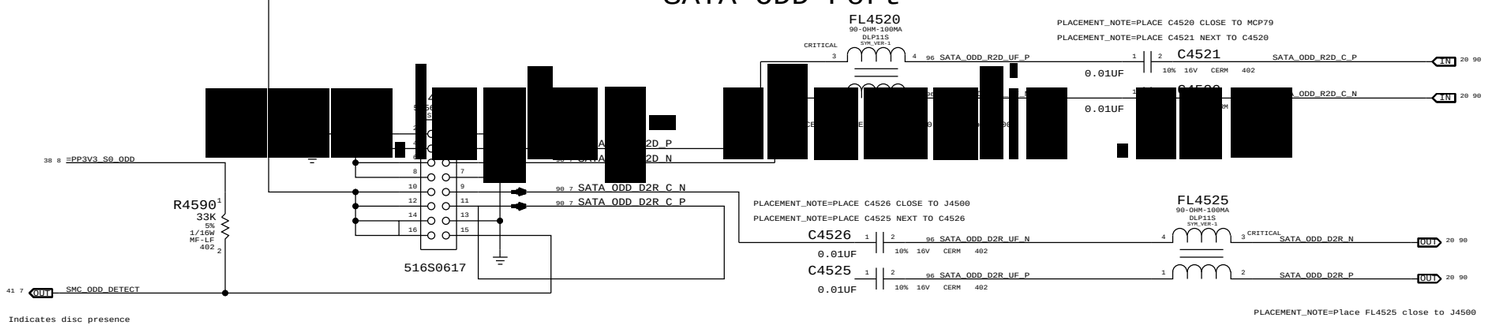
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 37 OF 98	

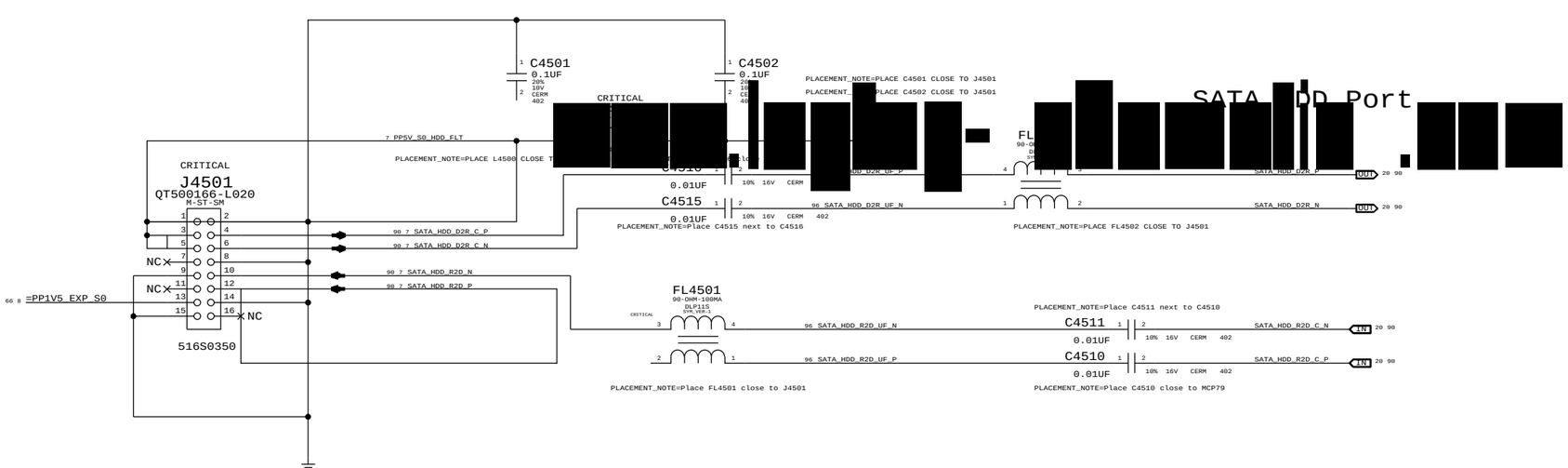
ODD Power Control



SATA ODD Port



SATA HDD Port



SATA Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

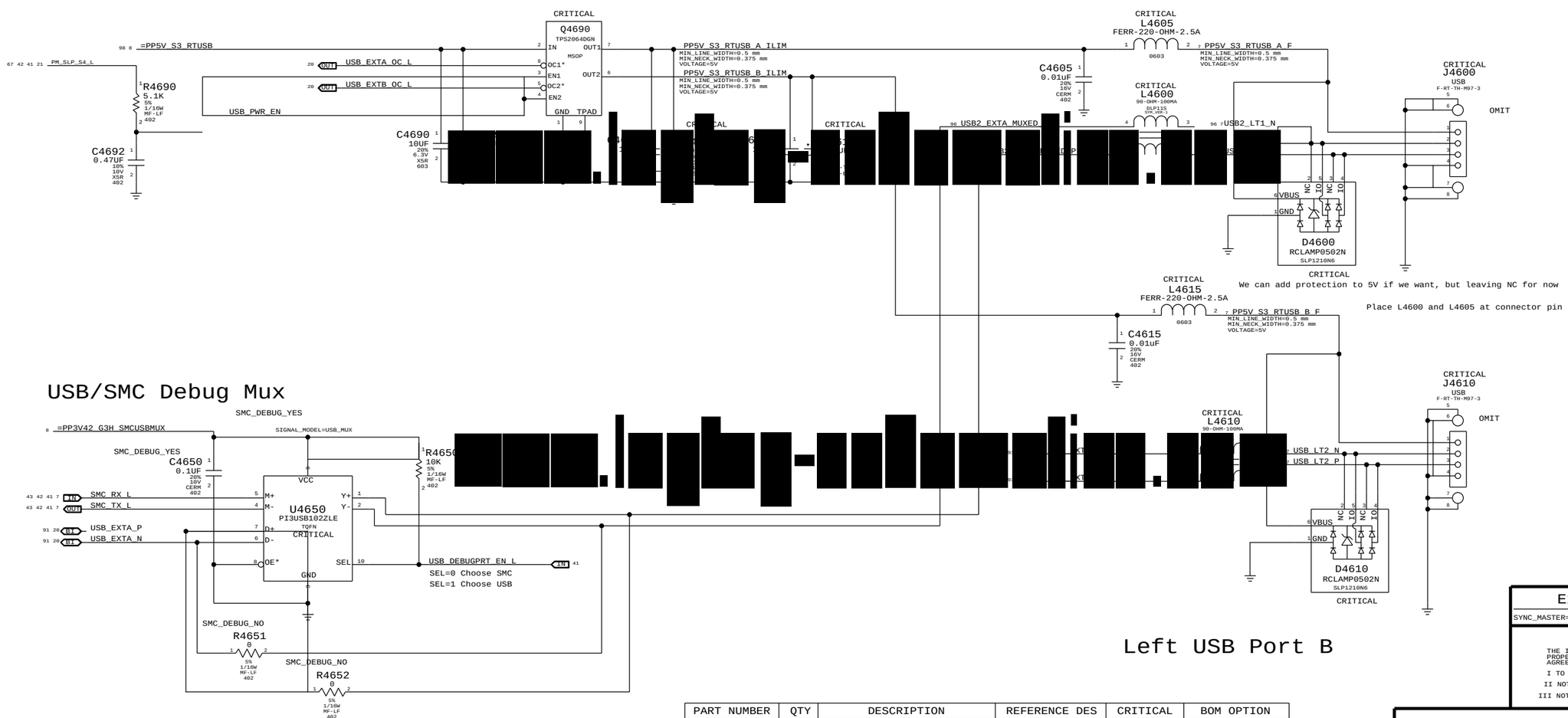
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 38 OF 98	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0638	2	CONN,RCPT,USB,HB,4P	J4600, J4610	CRITICAL	

External USB Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

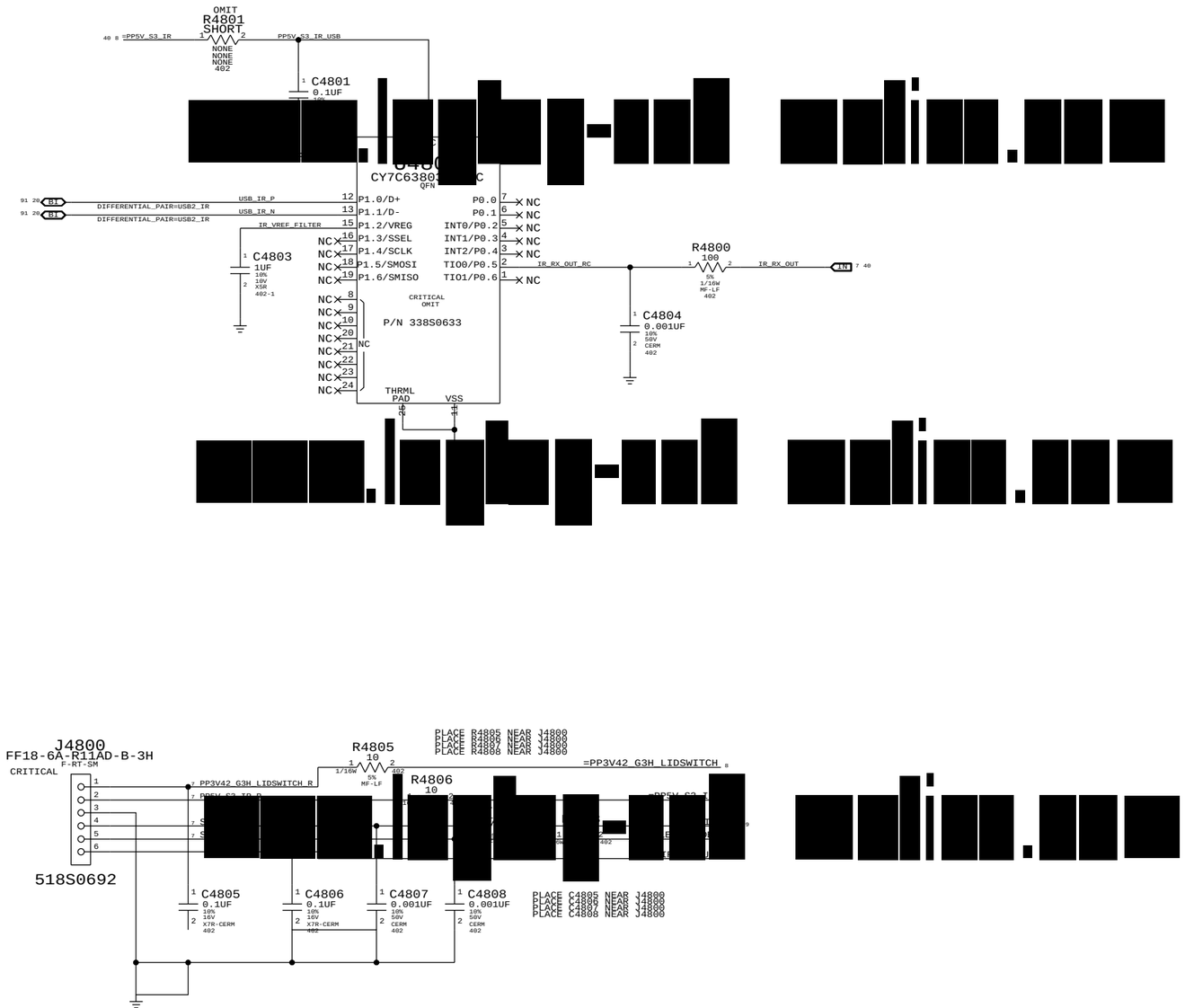
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 39 OF 98



Front Flex Support

SYNC_MASTER=CHANG_K20 SYNC_DATE=07/18/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

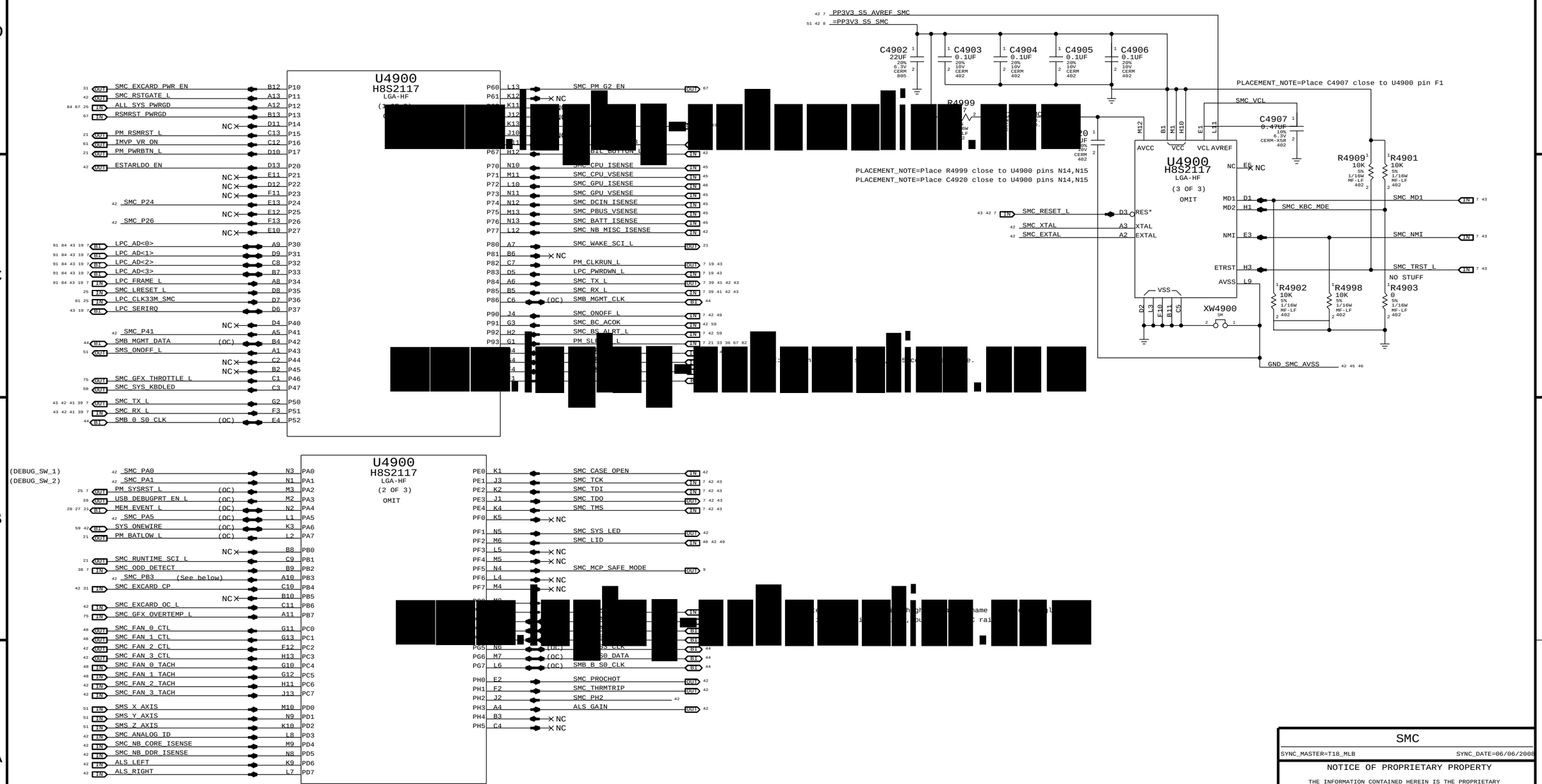
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 40 OF 98

NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SMC

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

NOTICE OF PROPRIETARY PROPERTY

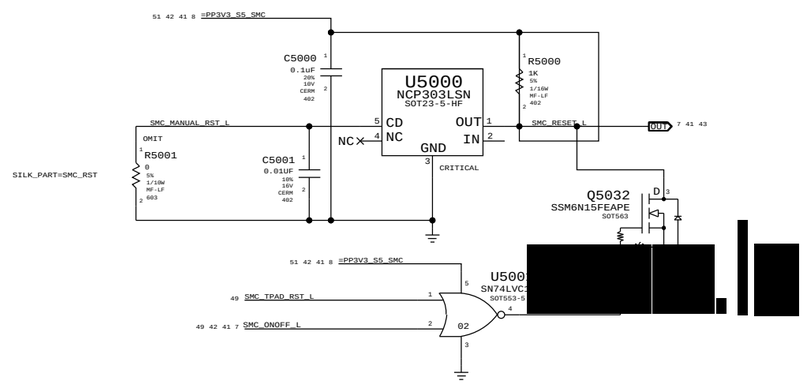
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

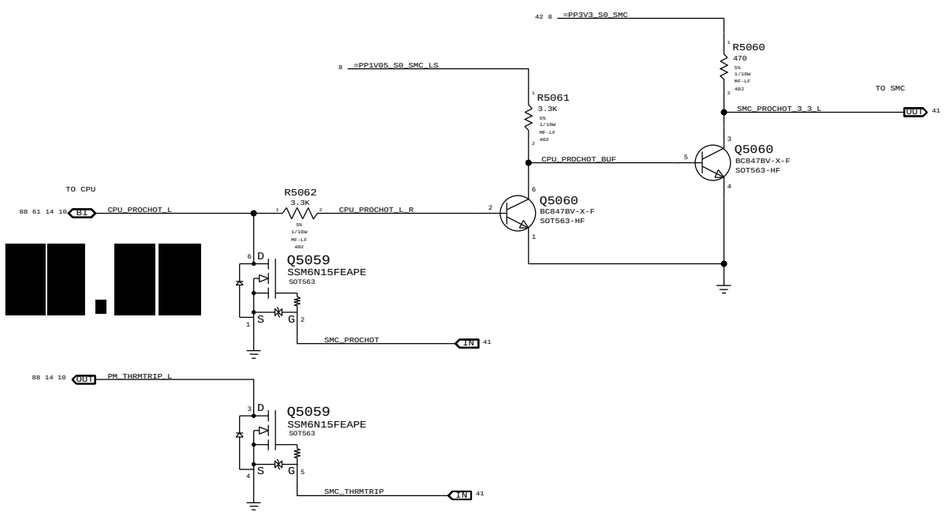
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 41 OF 98	

SMC Reset "Button" / Brownout Detect



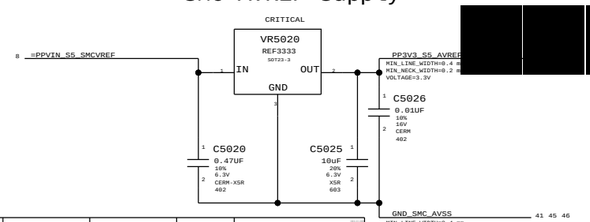
SMC FSB to 3.3V Level Shifting



41 SMC_FAN_2_CTL — NC_SMC_FAN_2_CTL 7 (MAKE_BASE=TRUE)
41 SMC_FAN_2_TACH — NC_SMC_FAN_2_TACH 7 (MAKE_BASE=TRUE)
41 SMC_FAN_3_CTL — NC_SMC_FAN_3_CTL 7 (MAKE_BASE=TRUE)
41 SMC_FAN_3_TACH — NC_SMC_FAN_3_TACH 7 (MAKE_BASE=TRUE)
41 ESTARLDO_EN — NC_ESTARLDO_EN 7 (MAKE_BASE=TRUE)
59 42 41 SMC_BC_ACOK (MAKE_BASE=TRUE) — =CHGR_ACOK 60
41 ALS_LEFT — SMC_MCP_VSENSE 45 (MAKE_BASE=TRUE)
41 ALS_RIGHT — SMC_CPU_HI_ISENSE (MAKE_BASE=TRUE)
SMC_NB_CORE_ISEN — SMC_MCP_CORE_ISENSE
SMC_NB_DDR — ISENSE
SMC_NB_MISC_ISEN — ISENSE
41 SMC_ANALOG_ID — SMC_GPU_1V8_ISENSE 46 (MAKE_BASE=TRUE)
41 SMC_P24 — TP_SMC_P24 (MAKE_BASE=TRUE)
41 SMC_P26 — SMC_BMON_MUX_SEL 45 (MAKE_BASE=TRUE)
41 SMC_P41 — TP_SMC_P41 7 (MAKE_BASE=TRUE)
41 ALS_GAIN — NC_ALS_GAIN 7 (MAKE_BASE=TRUE)
41 SMC_PB3 — SMC_IG_THROTTLE_L 21 (MAKE_BASE=TRUE)
41 SMC_RSTGATE_L — TP_SMC_RSTGATE_L (MAKE_BASE=TRUE)

41 OUT SMC_EXCARD_OC_L — R5095 0 5% 1/16W MF-LF 402 — EXCARD_OC_L IN 20 31

SMC AVREF Supply

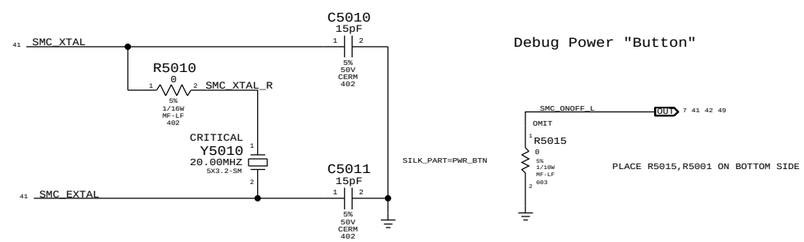


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

SMC [redacted] l Circuit

SMS_INT_L [redacted] =SM[redacted]

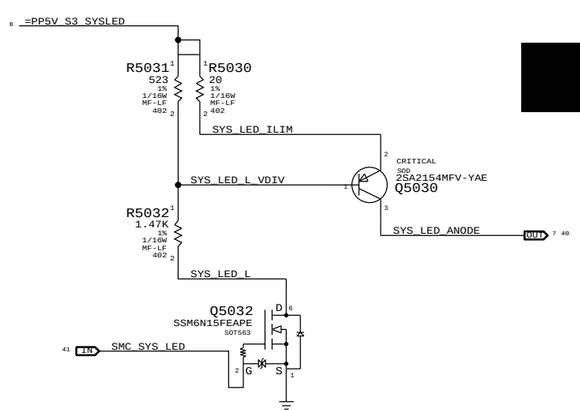
Debug Power "Button"



51 42 41 8 =PP3V3_S5_SMC

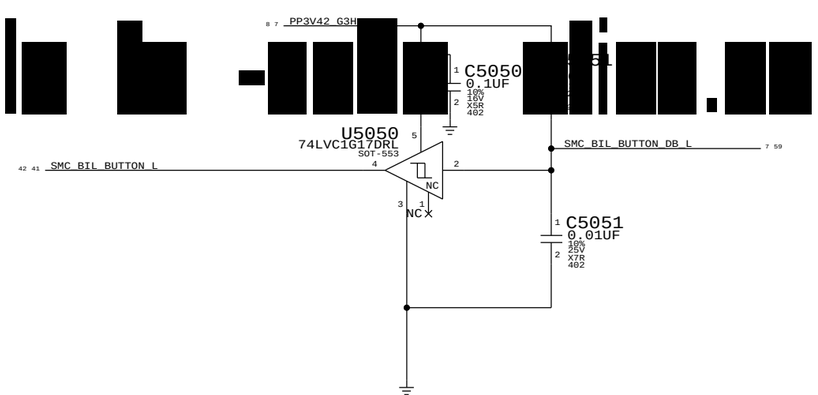
41 SMC_PA0	R5091	100K	5%	1/16W	MF-LF	402
41 SMC_PA1	R5092	100K	5%	1/16W	MF-LF	402
49 42 41 7 SMC_ONOFF_L	R5070	10K	5%	1/16W	MF-LF	402
49 41 40 SMC_LID	R5071	100K	5%	1/16W	MF-LF	402
41 SMC_PH2	R5072	10K	5%	1/16W	MF-LF	402
43 41 39 7 SMC_TX_L	R5073	10K	5%	1/16W	MF-LF	402
43 41 39 7 SMC_RX_L	R5074	100K	5%	1/16W	MF-LF	402
	ONEWIRE_PU					
59 41 SYS_ONEWIRE	R5075	2.0K	5%	1/16W	MF-LF	402
59 41 7 SMC_BS_ALRT_L	R5076	100K	5%	1/16W	MF-LF	402
43 41 7 SMC_TMS	R5077	10K	5%	1/16W	MF-LF	402
43 41 7 SMC_TDO	R5078	10K	5%	1/16W	MF-LF	402
43 41 7 SMC_TDI	R5079	10K	5%	1/16W	MF-LF	402
43 41 7 SMC_TCK	R5080	10K	5%	1/16W	MF-LF	402
42 41 SMC_BIL_BUTTON_L	R5081	10K	5%	1/16W	MF-LF	402
59 42 41 SMC_BC_ACOK	R5087	470K	5%	1/16W	MF-LF	402

System (Sleep) LED Circuit



[redacted]

8 7 PP3V42_G3H [redacted]



41 36 33 21 SMC_ADAPTER_EN — R5085 10K 5% 1/16W MF-LF 402
41 SMC_CASE_OPEN — R5086 10K 5% 1/16W MF-LF 402
41 31 SMC_EXCARD_CP — R5088 10K 5% 1/16W MF-LF 402
41 PM_SLP_S5_L
67 41 39 21 PM_SLP_S4_L — R5090 100K 5% 1/16W MF-LF 402

42 8 =PP3V3_S0_SMC
41 SMC_PA5 — R5089 10K 5% 1/16W MF-LF 402

SMC Support

SYNC_MASTER=M98_MLB — SYNC_DATE=05/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

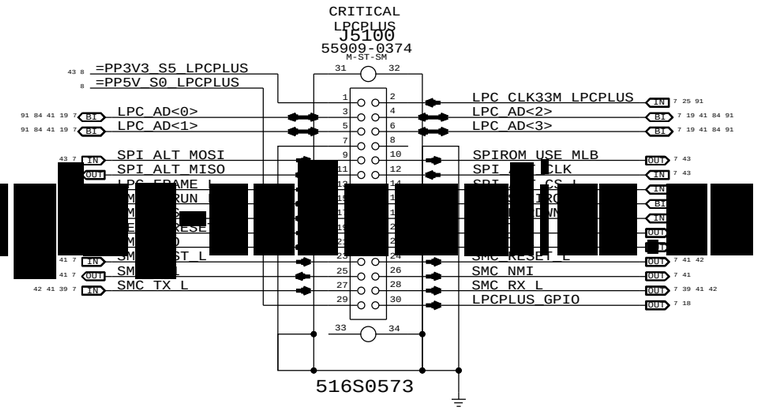
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

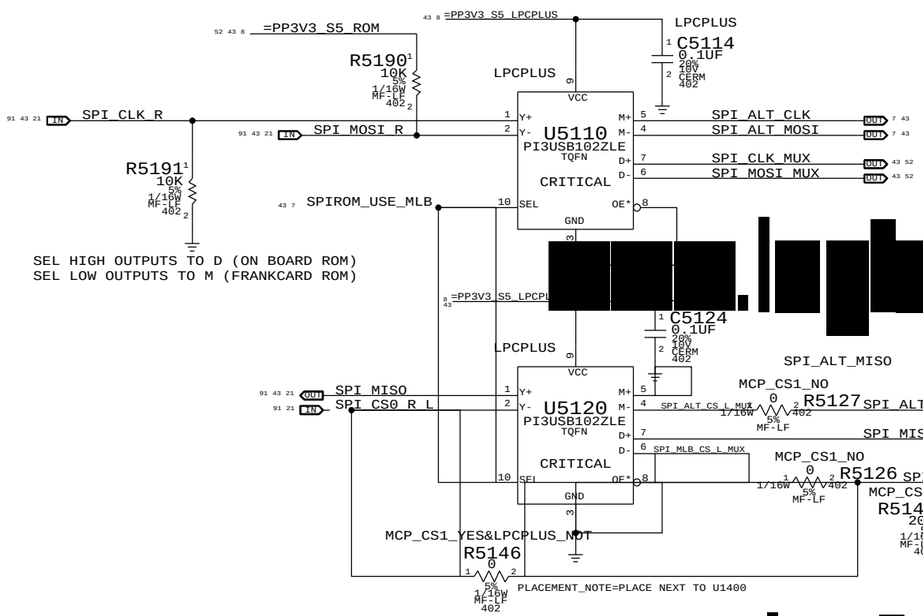
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 42 OF 98	

LPC+SPI Connector



Alternate SPI ROM [redacted]

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP

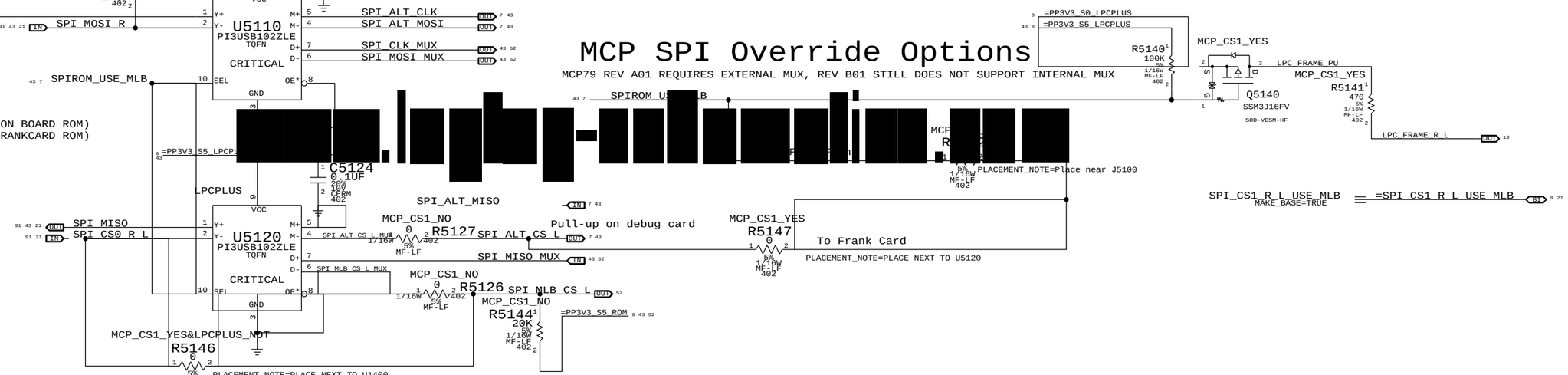


MCP79 Internal SPI MUX Support

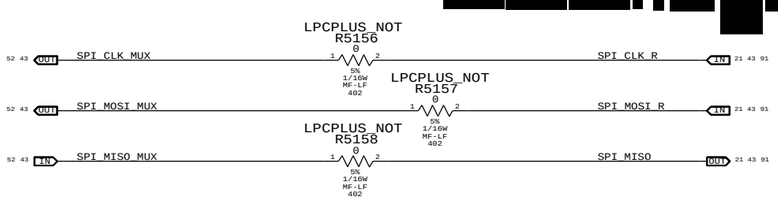
NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON

MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX



SPI MUX BY[redacted]



LPC+SPI Debug Connector

SYNC_MASTER=CHANG_K20 SYNC_DATE=05/28/2008

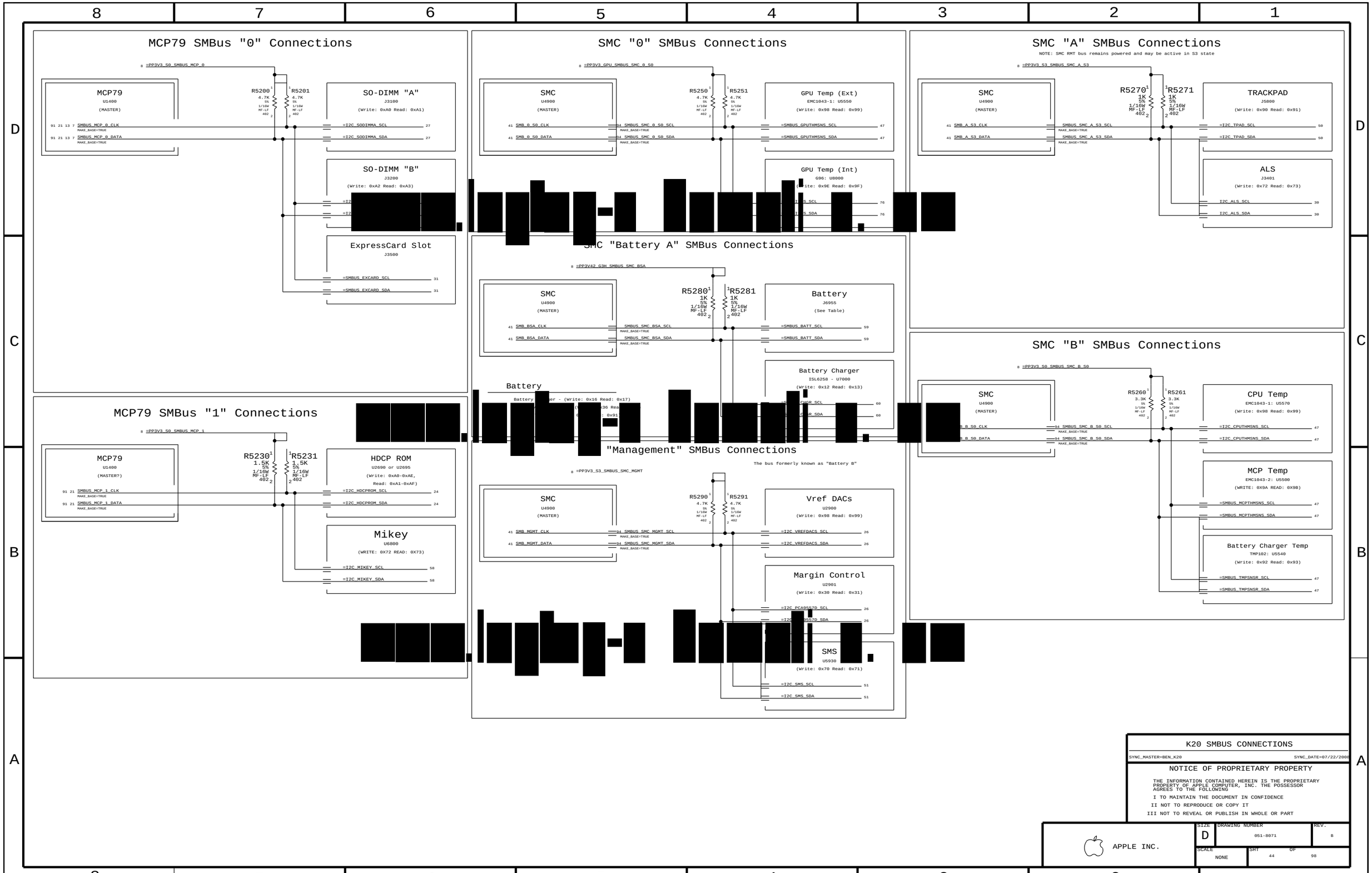
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 43 OF 98	



K20 SMBUS CONNECTIONS

SYNC_MASTER=BEN_K20 SYNC_DATE=07/22/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

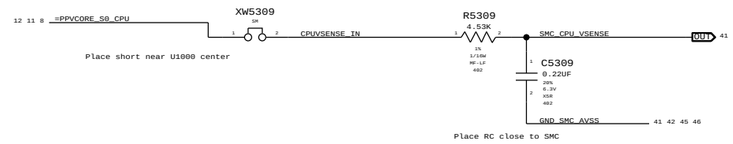
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

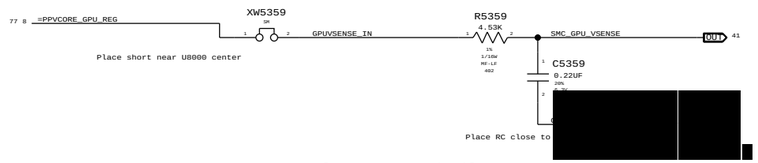
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 44 OF 98	

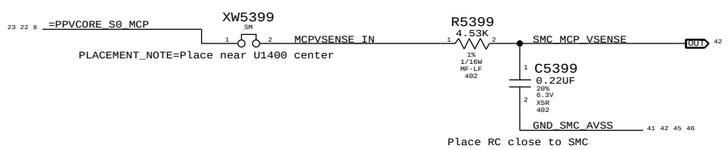
CPU Voltage Sense / Filter



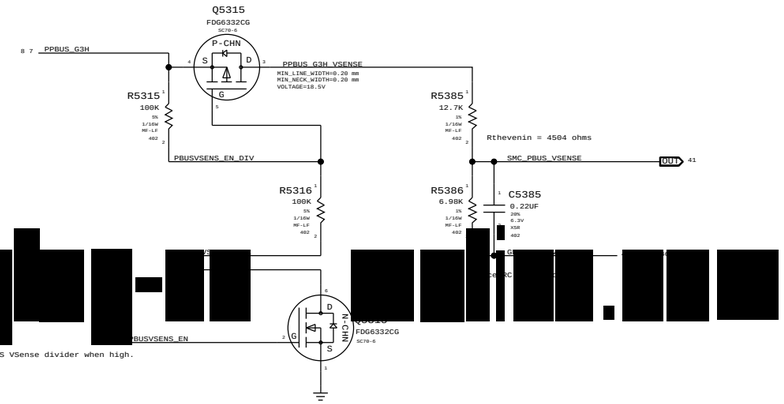
GPU Voltage Sense / Filter



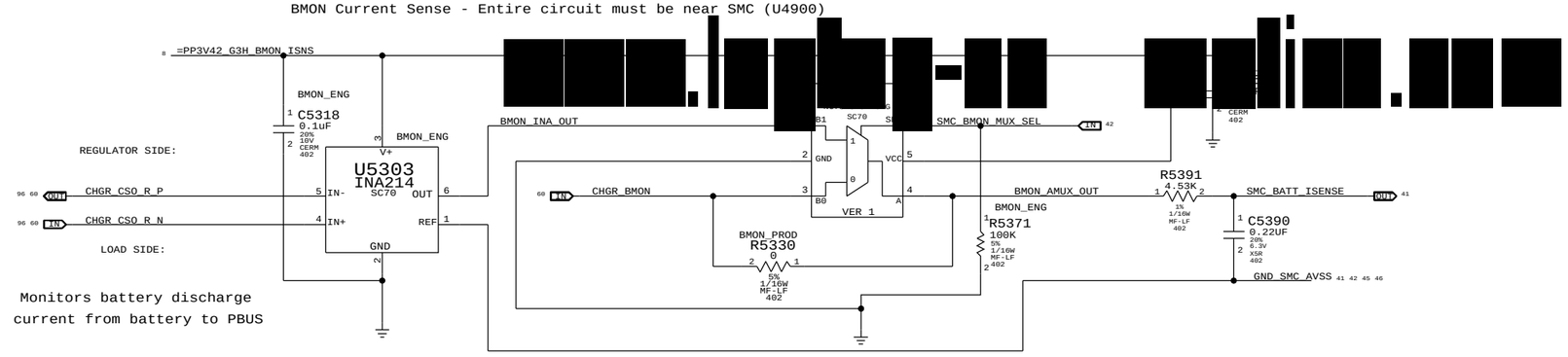
MCP Voltage Sense / Filter



PBUS Voltage Sense & Filter



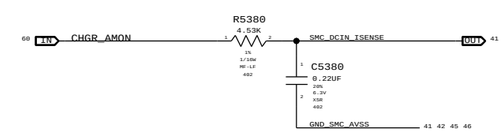
BMON Current Sense - Entire circuit must be near SMC (U4900)



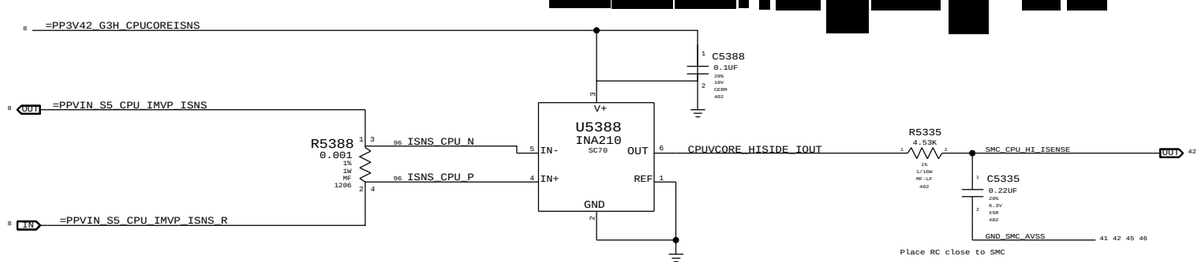
INA214 has gain of 100V/V
U5303 only senses current up to 6.6A

DCIN Current Sense Filter

Place RC close to SMC



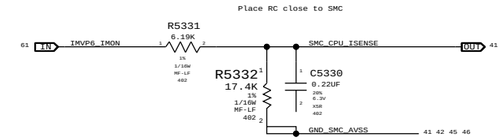
CPU VCore [redacted]



Consider INA211 (GAIN 500 version) since I=4.93 Amps across R5388

CPU VCore Load Side Current Sense / Filter

Place RC close to SMC



Current & Voltage Sensing

SYNC_MASTER=YWU_K20 SYNC_DATE=08/20/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

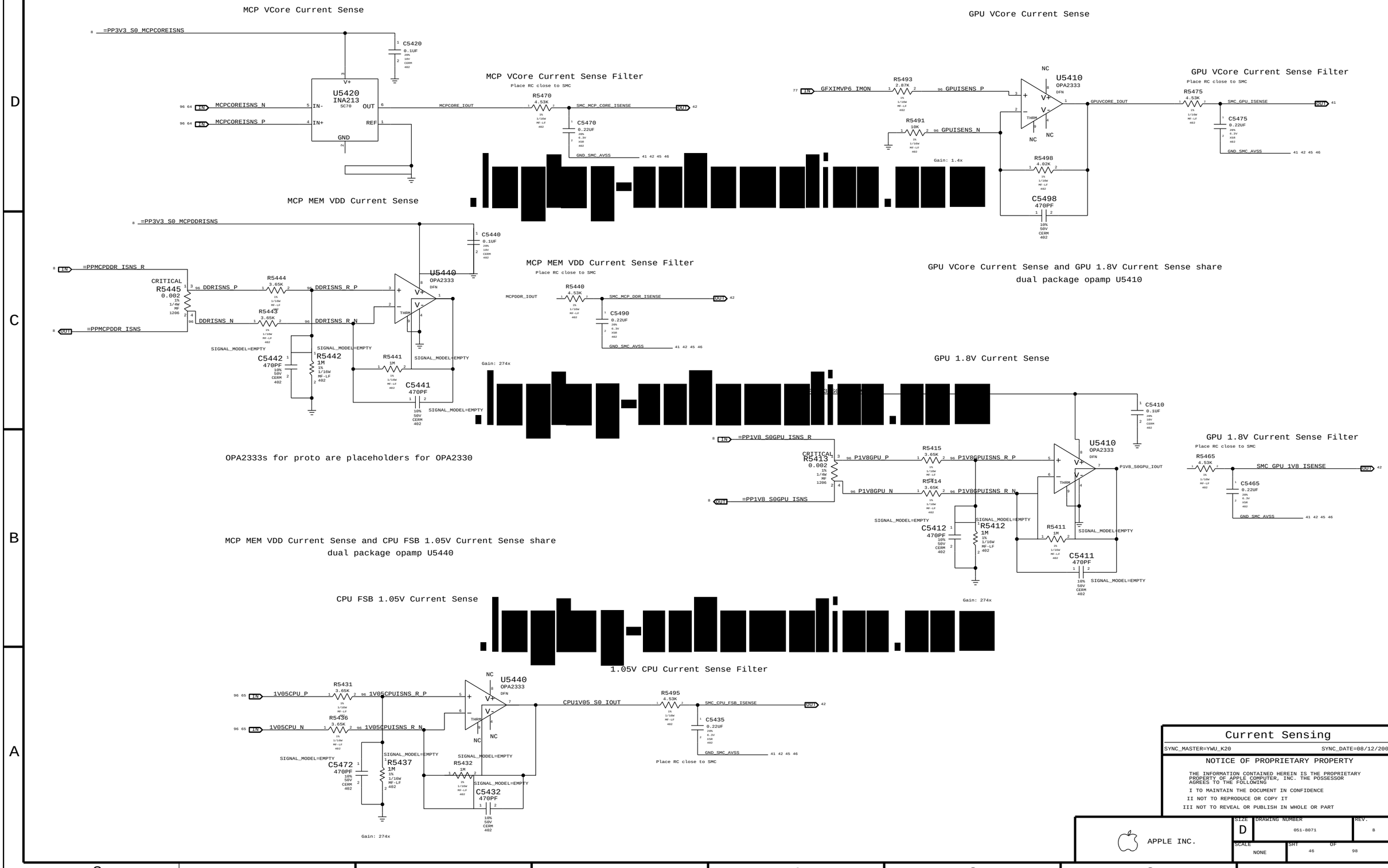
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 45 OF 98	



Current Sensing

SYNC_MASTER=YWU_K20 SYNC_DATE=08/12/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

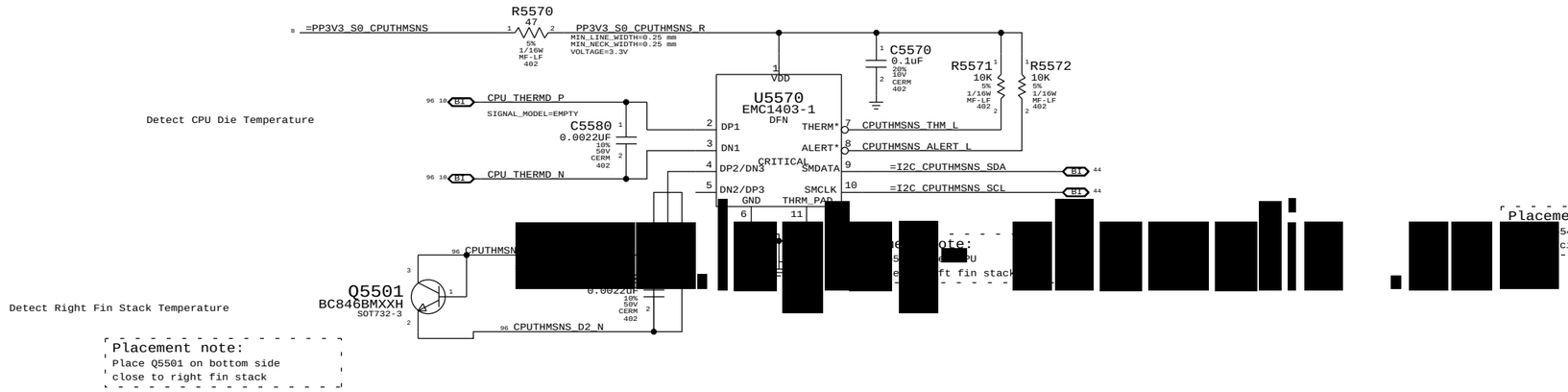
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

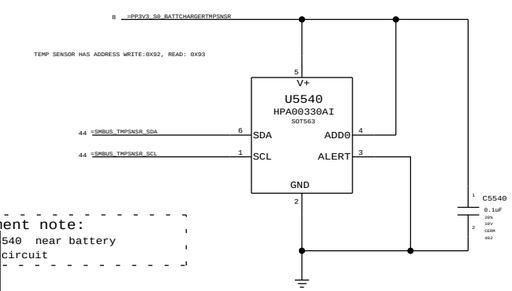
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 46 OF 98	

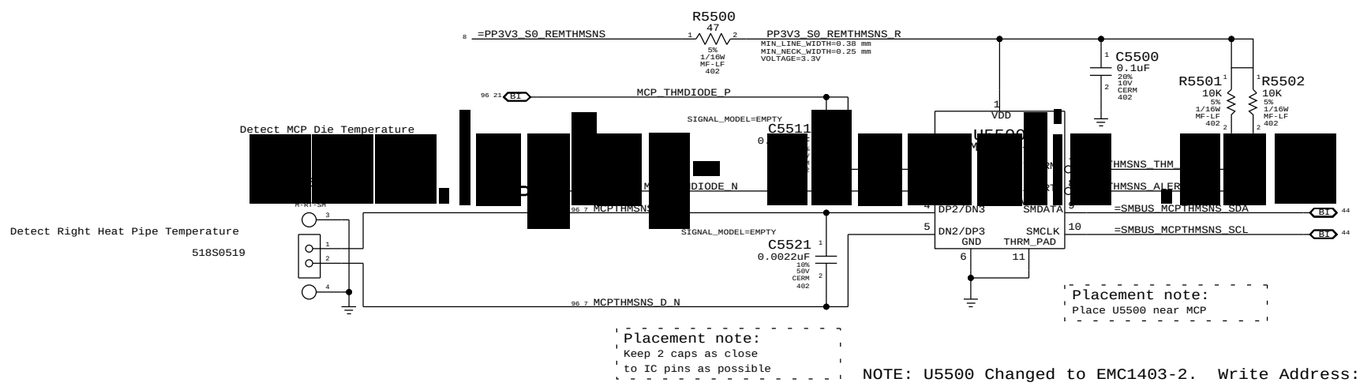
CPU Proximity/CPU Die/Right Fin Stack



Battery Charger Proximity



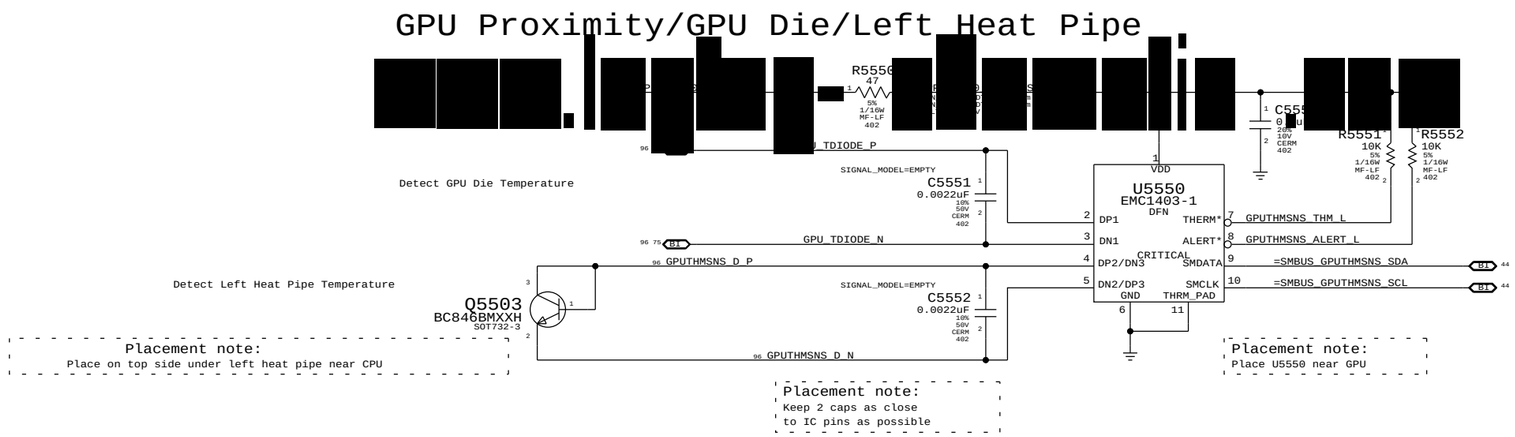
MCP Proximity/MCP Die/Right Heat Pipe



Note: EMC1403 can perform Beta
Compensation for External Diode 1 only

NOTE: U5500 Changed to EMC1403-2. Write Address: 0x9A

GPU Proximity/GPU Die/Left Heat Pipe



Thermal Sensors

SYNC_MASTER=YWU_K20 SYNC_DATE=05/28/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

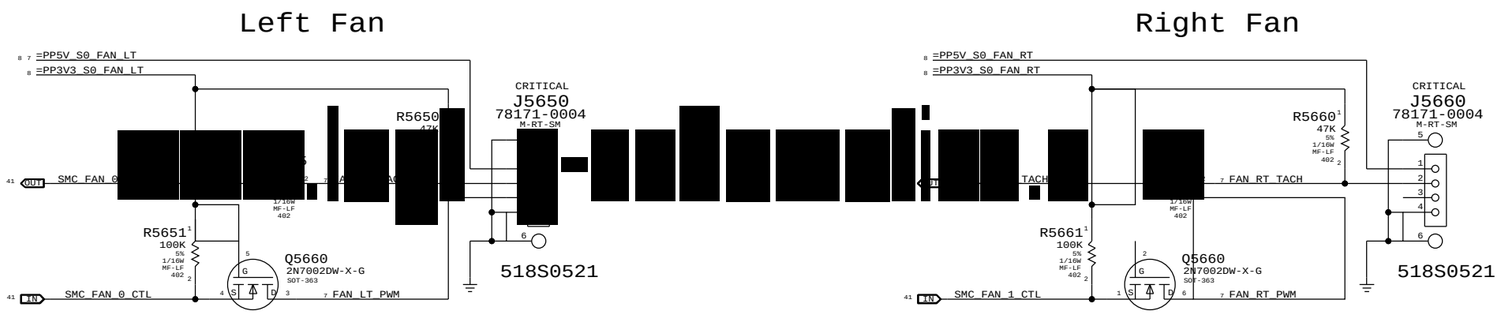
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 47 OF 98	



Fan Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 48 OF 98	

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

PSOC USB CONTROLLER

USB INTERFACES TO MLB
SPI HOST TO Z2

TRACKPAD PICK BUTTONS
KEYBOARD SCANNER

PP3V3_S3_PSOC

PICKB_L
BUTTON_DISABLE
Z2_HOST_INTN
WS_LEFT_SHIFT_KEY
WS_LEFT_OPTION_KEY

CRITICAL
U5701
CY8C24794
MLF
(SYM-VER2)
APN 337S2983
OMIT

WS_CONTROL_KEY
Z2_KEY_ACT_L
Z2_BOOT_CFG1
TP_P4_5
Z2_DEBUG3
Z2_RESET
PSOC_MISO
PSOC_F_CS_L
PSOC_MOSI
PSOC_SCLK
Z2_MISO
Z2_CS_L
Z2_MOSI
Z2_SCLK

WS_KBD16N
WS_KBD15_C
WS_KBD14
WS_KBD13
WS_KBD12
WS_KBD11
WS_KBD10
WS_KBD9
WS_KBD8
WS_KBD7
WS_KBD1
WS_KBD2
WS_KBD3
WS_KBD4
WS_KBD5
WS_KBD6

THRML PAD

TP_PSOC_SCL
TP_PSOC_SDA
TP_PSOC_P1_3
ISSP_SCLK_P1_1
ISSP SCLK/I2C SCL
TP_P7_7

DIFFERENTIAL_PAIR=USB2_TPAD
USB_TPAD_P — R5701 24 5% 1/16W MF-LF 402 — USB_TPAD_R_P
NET_SPACING_TYPE=USB
NET_PHYSICAL_TYPE=USB_90D

TO MLB CONNECTOR

USB_TPAD_N — R5702 24 5% 1/16W MF-LF 402 — USB_TPAD_R_N

U5701 CHIP DECOUPLING

PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

PP3V3_S3_PSOC — MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM — R5704 1.5 5% 1/16W MF-LF 402 — =PP3V3_S3_TPAD

C5701 4.7UF 20% 6.3V X5R 603
C5702 100PF 5% 50V CERM 402
C5703 0.1UF 10% 16V X7R-CERM 402
C5704 100PF 5% 50V CERM 402
C5705 0.1UF 10% 16V X7R-CERM 402
C5706 4.7UF 20% 6.3V X5R 603

KEYBOARD CONNECTOR

CRITICAL
J5713
APN 518S0637

=PP3V3_S3_TPAD
WS_KBD1
WS_KBD2
WS_KBD3
WS_KBD4
WS_KBD5
WS_KBD6
WS_KBD7
WS_KBD8
WS_KBD9
WS_KBD10
WS_KBD11
WS_KBD12
WS_KBD13
WS_KBD14
WS_KBD15_CAP
WS_KBD16_NUM
WS_KBD17
WS_KBD18
WS_KBD19
WS_KBD20
WS_KBD21
WS_KBD22
WS_KBD23
WS_KBD_ONOFF_L
=PP3V42_G3H_TPAD
WS_LEFT_SHIFT_KBD
WS_LEFT_OPTION_KBD
WS_CONTROL_KBD

F-RT-SM
FF14-30A-R11B-B-3H

R5714 470 1% 1/16W MF-LF 402
R5715 10K 1% 1/16W MF-LF 402
R5710 1K 5% 1/16W MF-LF 402

SMC_ONOFF_L
C5710 0.1UF 20% 10V CERM 402
PLACEMENT_NOTE=NEAR J5713

=PP3V3_S3_TPAD
ISSP_SCLK_P1_1 — ISSP CLOCK
ISSP_SDATA_P1_0 — ISSP DATA

ISOLATION CIRCUIT

=PP3V42_G3H_TPAD
WS_LEFT_SHIFT_KBD

C5726 0.1UF 20% 10V CERM 402
=PP3V42_G3H_TPAD
=PP3V3_S3_TPAD
WS_LEFT_OPTION_KBD
CRITICAL
U5726 TC7S208AFEAPE SOT665
WS_LEFT_OPTION_KEY

C5727 0.1UF 20% 10V CERM 402
=PP3V42_G3H_TPAD
WS_CONTROL_KEY

SMC_MANUAL_RESET LOGIC

=PP3V42_G3H_TPAD
C5758 0.1UF 10% 16V X7R-CERM 402

APN 311S0406
CRITICAL
U5703 SN74LVC1G10 SC70

WS_LEFT_SHIFT_KBD
WS_LEFT_OPTION_KBD
WS_CONTROL_KBD
SMC_TPAD_RST_L

R5769 33K 5% 1/16W MF-LF 402
R5770 33K 5% 1/16W MF-LF 402
R5771 33K 5% 1/16W MF-LF 402

TPAD BUTTONS DISABLE

BUTTON_DISABLE

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

Q5701
SSM3K15FV
SOD-VESM-HF

SMC_LID

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

WELLSPRING 1

SYNC_MASTER=YMA_K20 SYNC_DATE=05/19/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

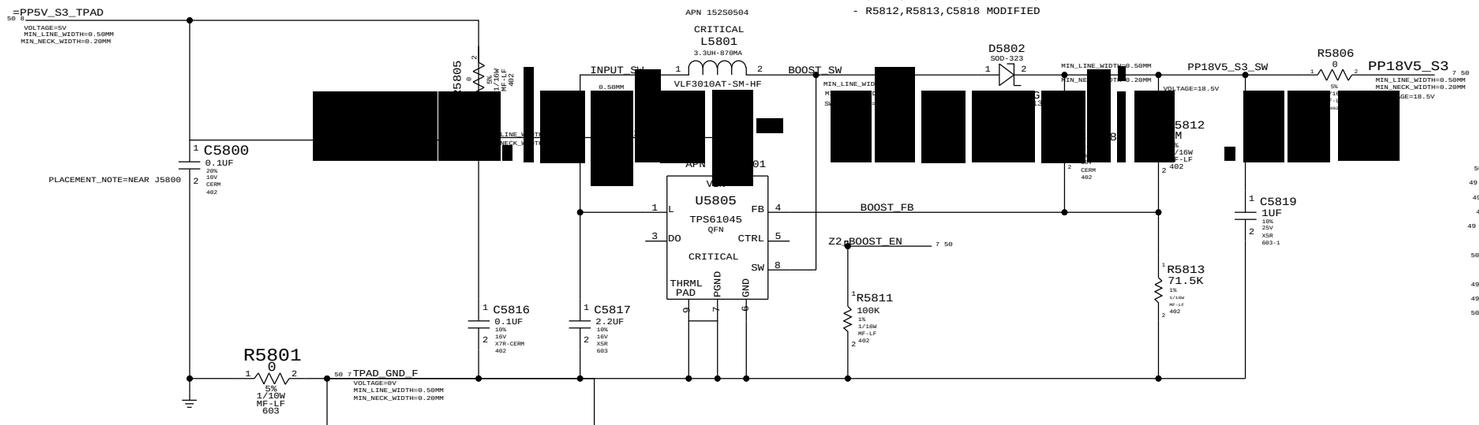
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

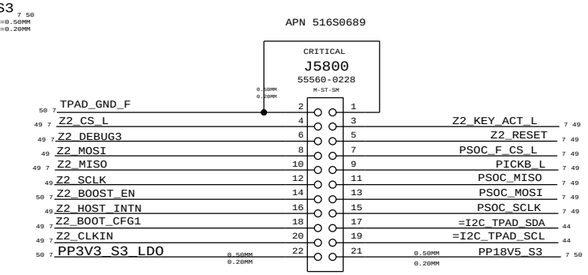
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 49 OF 98	

BOOSTER +18.5VDC FOR SENSORS

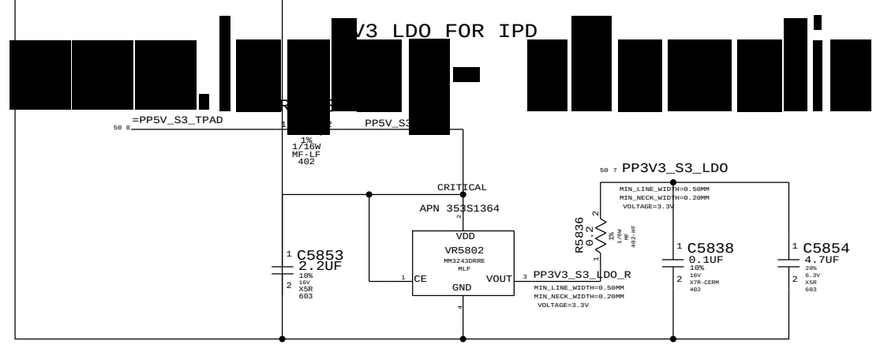
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



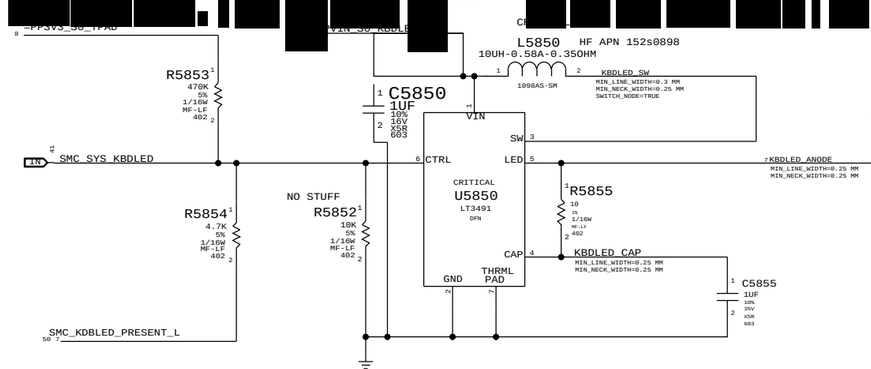
IPD FLEX CONNECTOR



[redacted]V3 LDO FOR IPD



[redacted]eyboard L[redacted]



To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

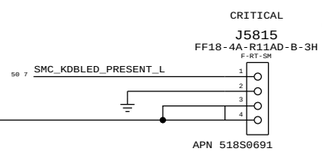
LOW = keyboard backlight present

HIGH= keyboard backlight not present

BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT

J5815 pin 1 is grounded on keyboard backlight flex



KBD BACKLIGHT CONNECTOR

WELLSPRING 2

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

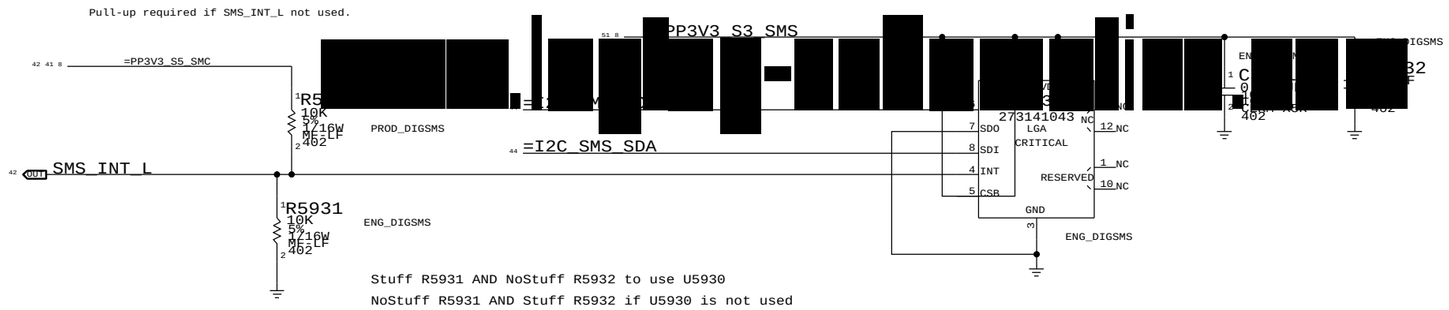
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

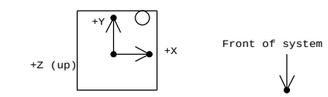
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 50 OF 98	

Digital SMS



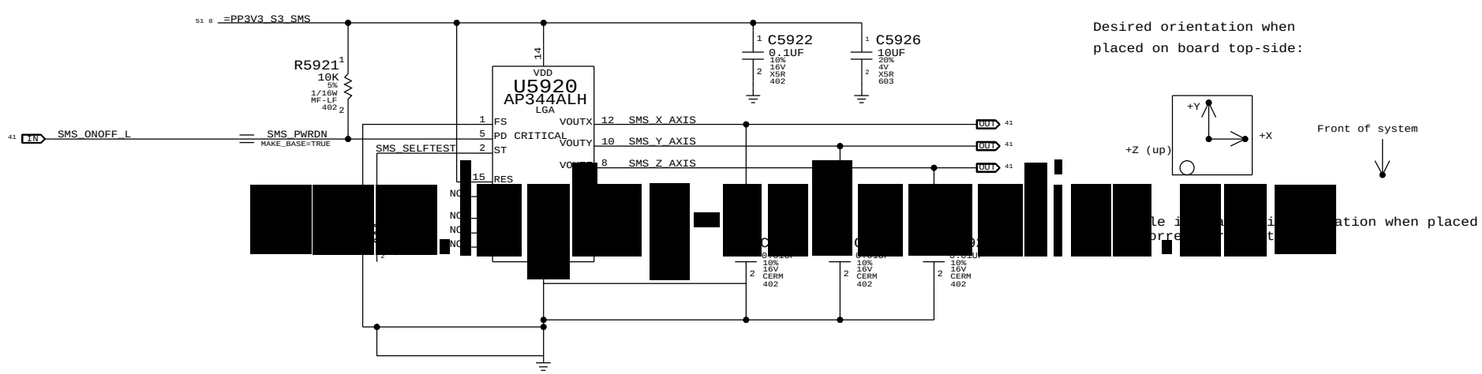
Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation

Sudden Motion Sensor (SMS)

SYNC_MASTER=YWU_K20 SYNC_DATE=06/17/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

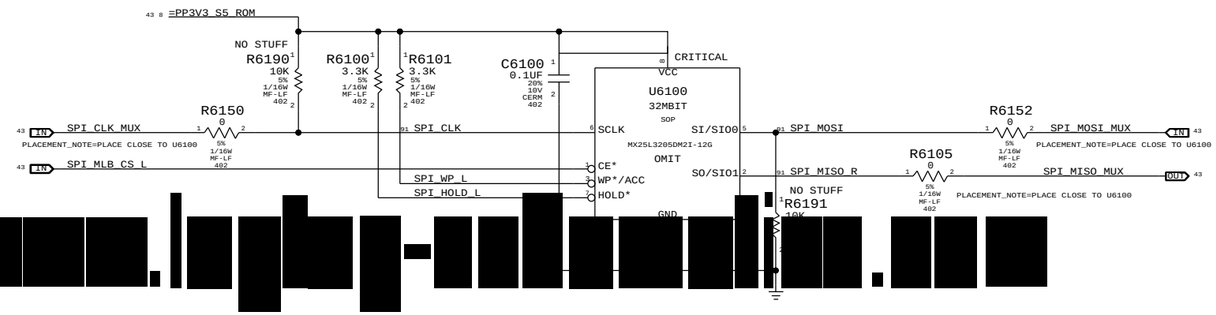
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 51 OF 98	



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with [redacted] R51
Any o[redacted]ele[redacted]
with [redacted]01

SPI ROM	
SYNC_MASTER=M98_MLB	SYNC_DATE=05/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

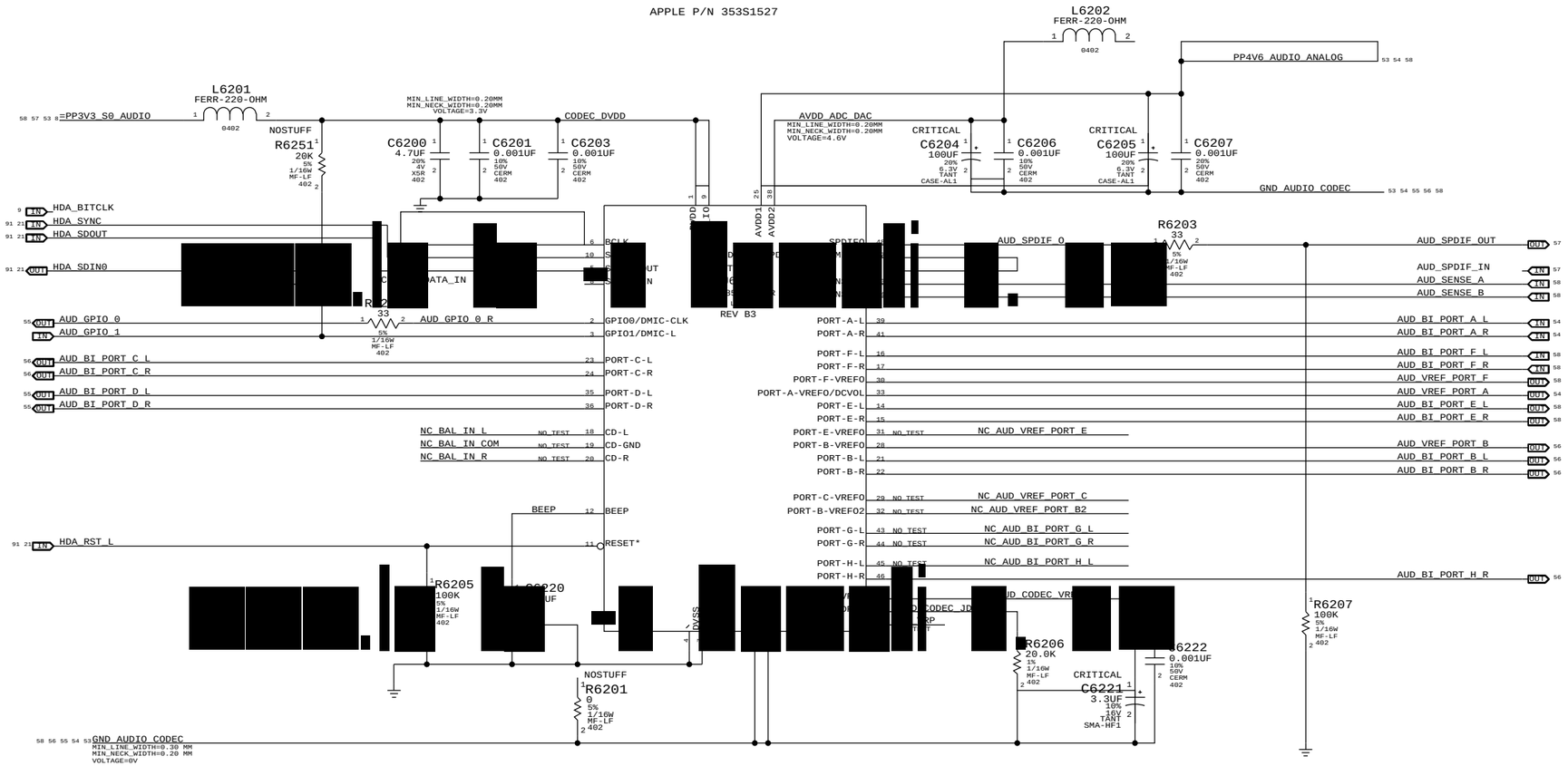
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 52 OF 98	

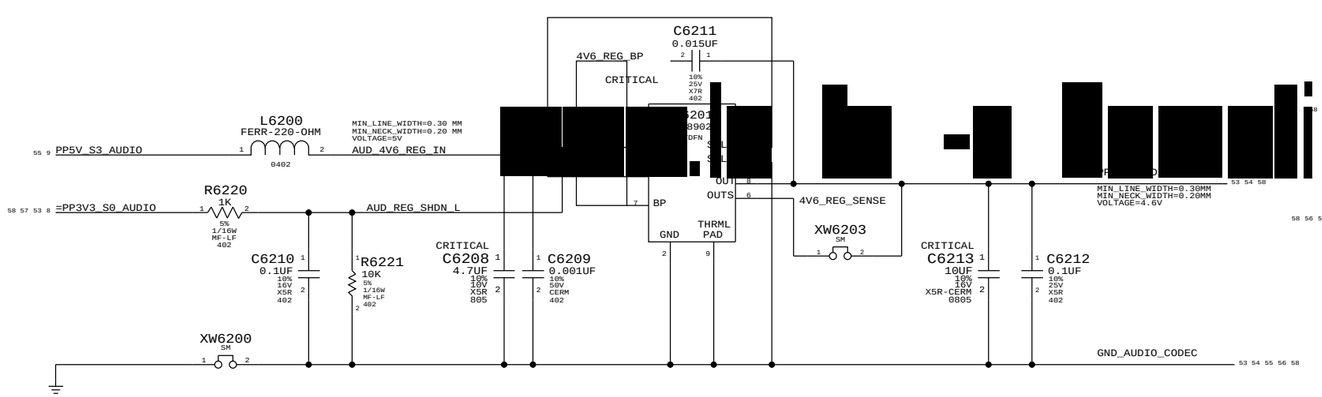
AUDIO CODEC

APPLE P/N 353S1527



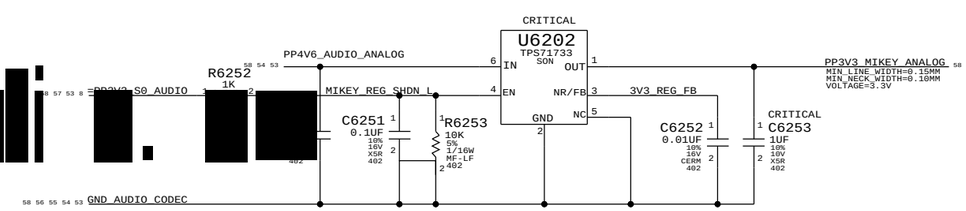
AUDIO 4.6 V REGULATOR

APPLE P/N 353S1897



MIKEY 3.3 V REGULATOR

APPLE P/N 353S1860



AUDIO:CODEC

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

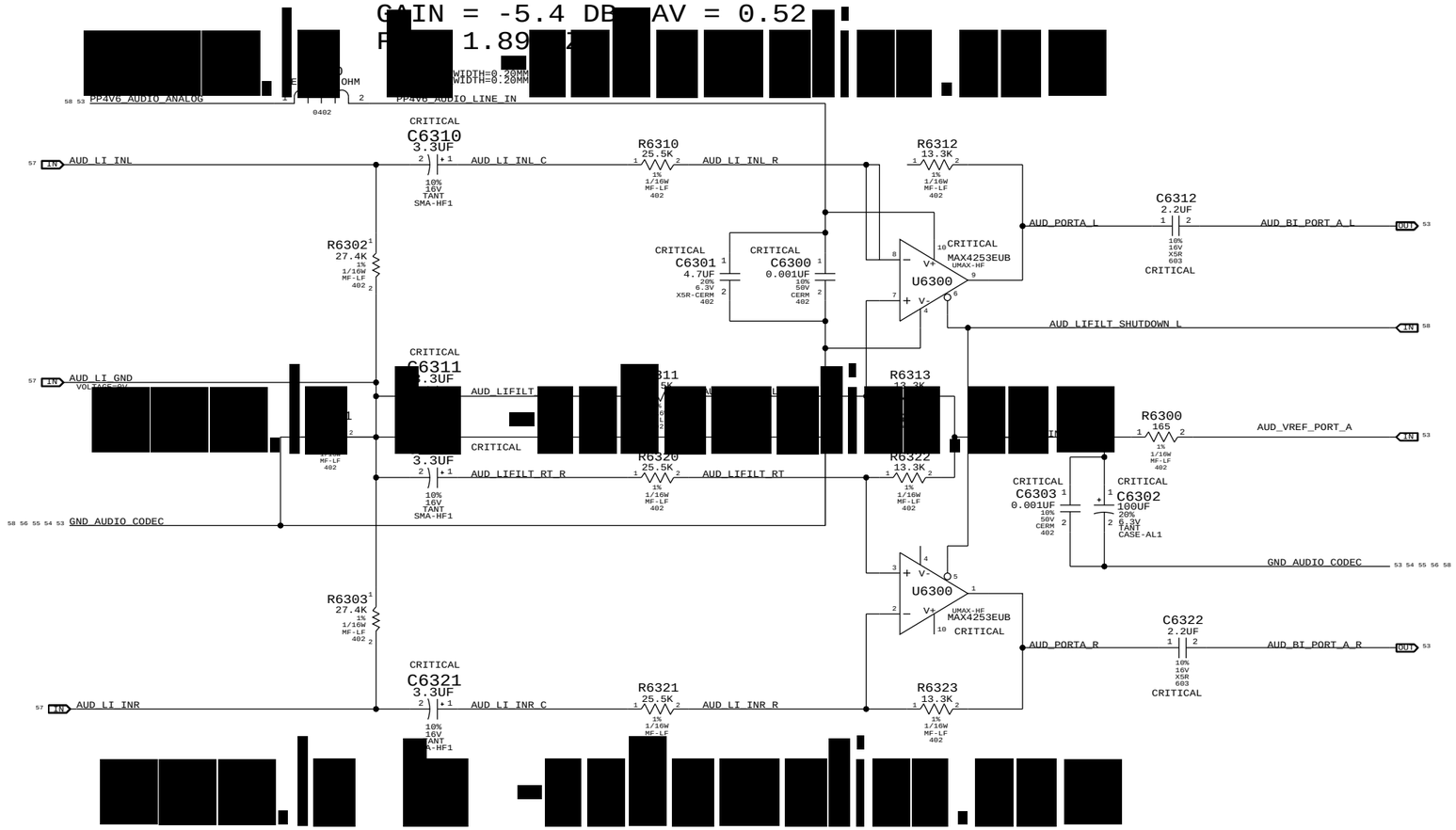
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 53 OF 98	

Pseudo-Diff Line-In Filter

GAIN = -5.4 DB [redacted] AV = 0.52 [redacted]

F[redacted] 1.89[redacted]



[redacted]

AUDIO: LINE IN	
SYNC_MASTER=AUDIO_K20	SYNC_DATE=09/29/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

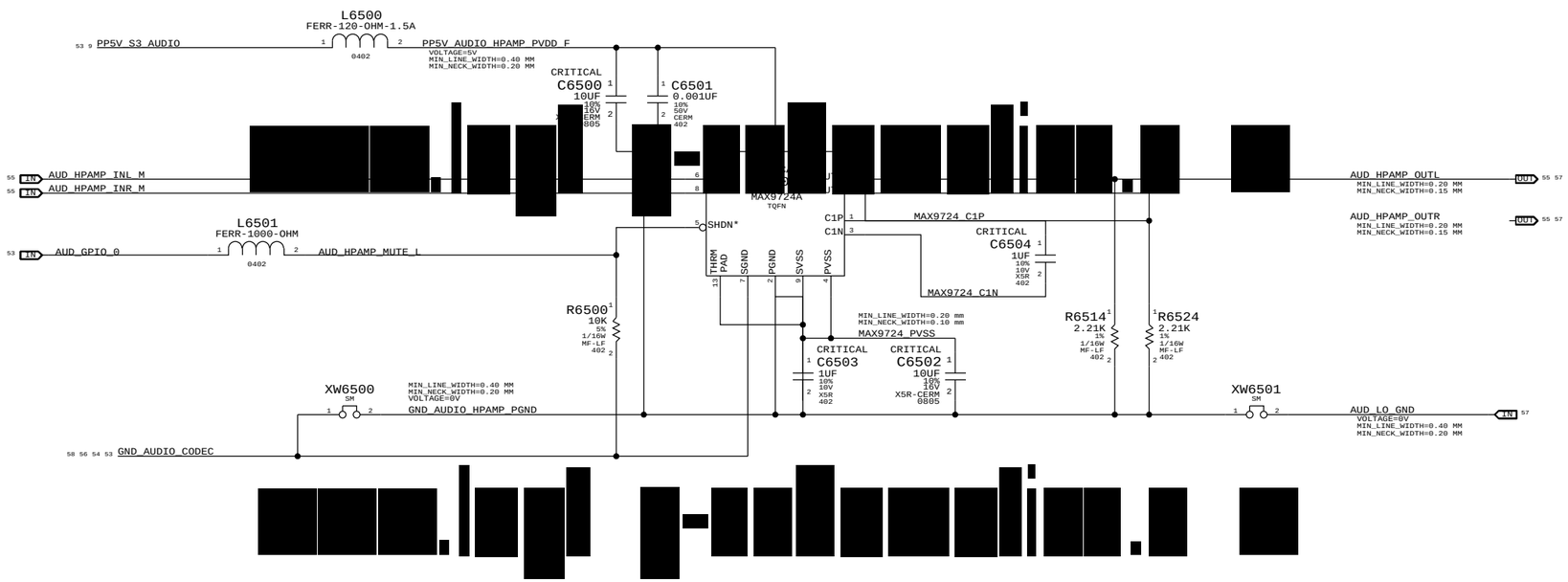
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 54 OF 98	

Headphone Amplifier (MAX9724A)

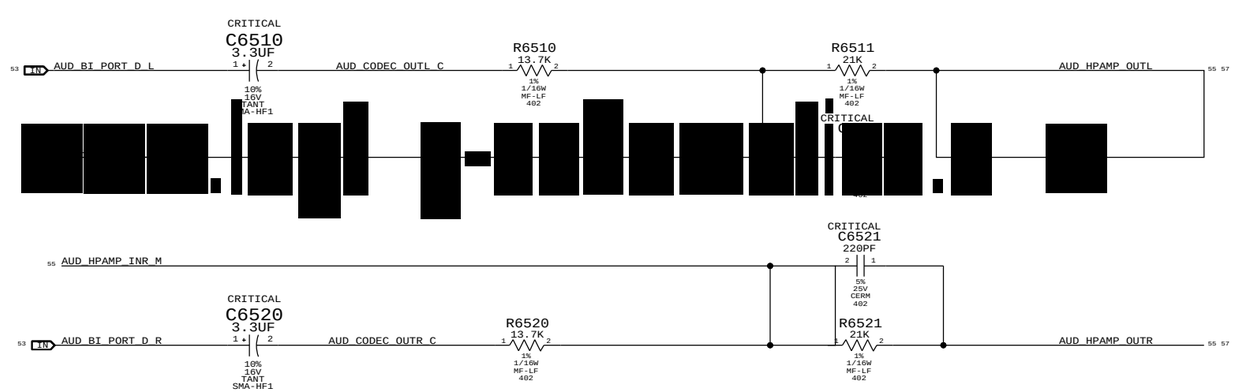
APN:353S1637



1st Order DAC Filter

HP:3.52 HZ LP:34 KHZ

VOLTAGE GAIN:1.53



AUDIO: HEADPHONE AMP

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

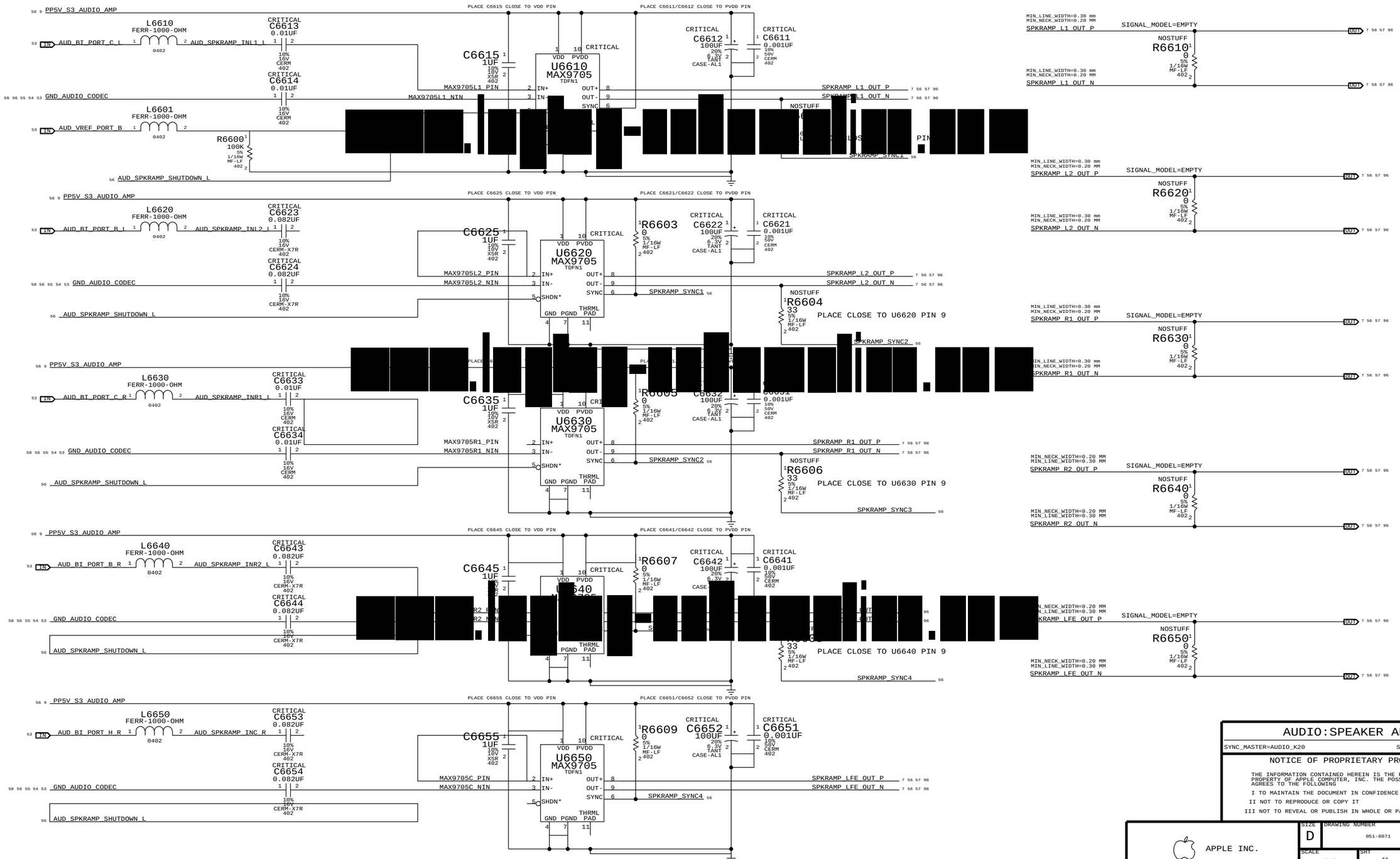
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 55 OF 98	

4X MONO SPEAKER AMPLIFIERS (MAX9705)
APN: 353S1595
GAIN = 12 DB

FC (SPEAKERS L1/R1) = ~796 HZ
FC (SPEAKERS L2/R2/LFE) = ~97 HZ

SPEAKER CHECKPOINTS



AUDIO:SPEAKER AMP

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

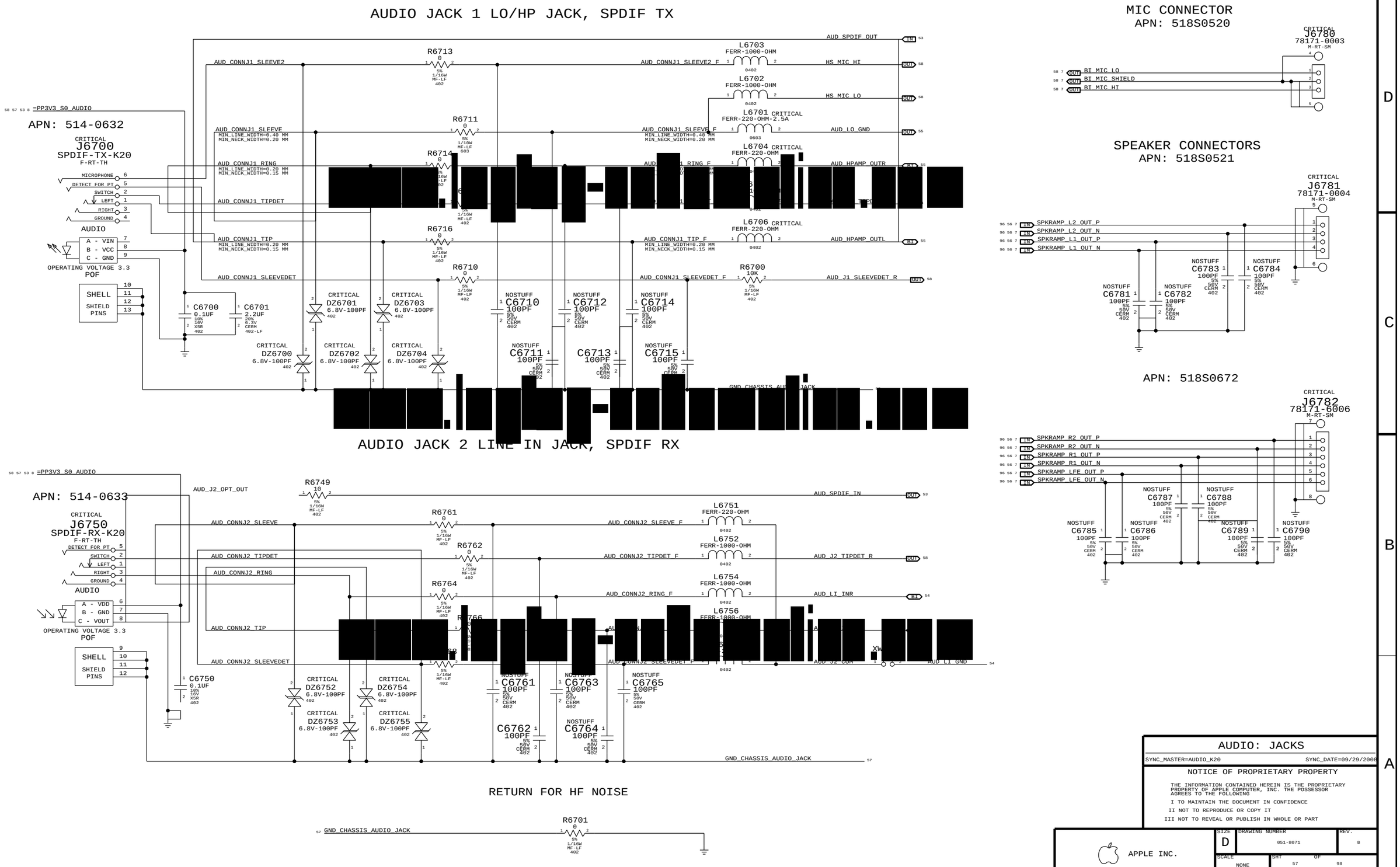
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 56 OF 98	



AUDIO: JACKS

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

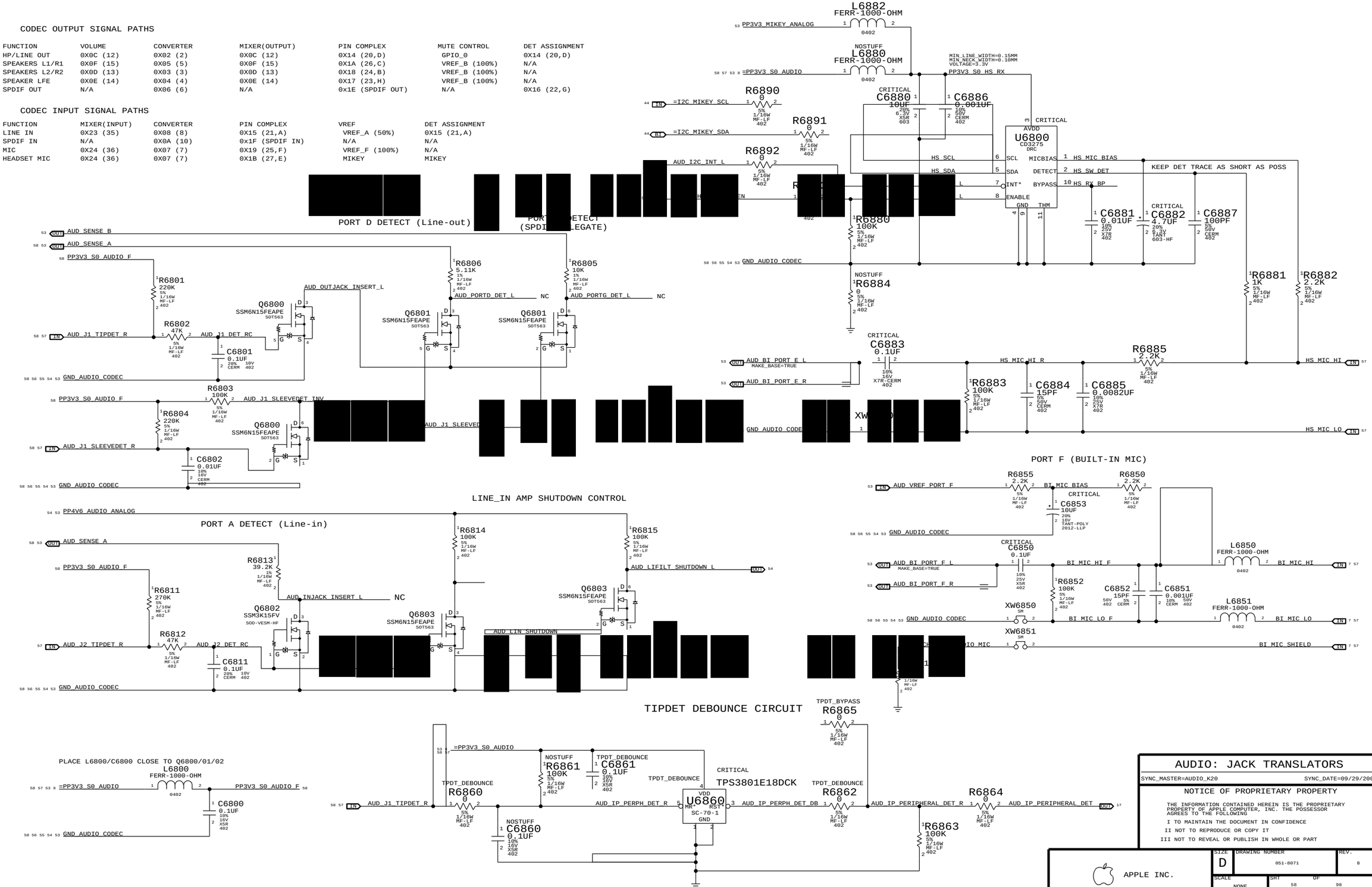
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 57 OF 98	

CODEC OUTPUT SIGNAL PATHS

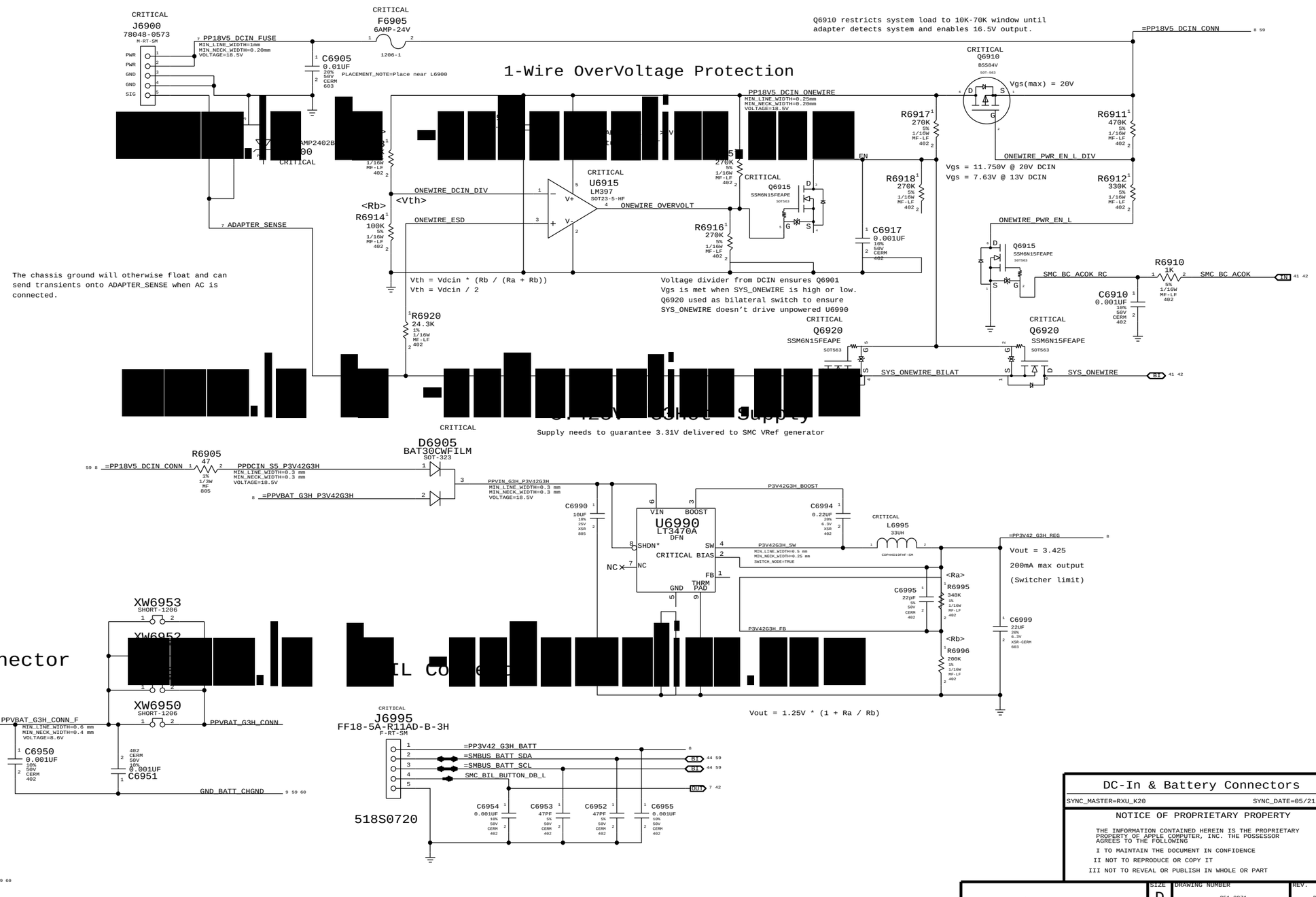
FUNCTION	VOLUME	CONVERTER	MIXER(OUTPUT)	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X0C (12)	0X02 (2)	0X0C (12)	0X14 (20,D)	GPIO_0	0X14 (20,D)
SPEAKERS L1/R1	0X0F (15)	0X05 (5)	0X0F (15)	0X1A (26,C)	VREF_B (100%)	N/A
SPEAKERS L2/R2	0X0D (13)	0X03 (3)	0X0D (13)	0X18 (24,B)	VREF_B (100%)	N/A
SPEAKER LFE	0X0E (14)	0X04 (4)	0X0E (14)	0X17 (23,H)	VREF_B (100%)	N/A
SPDIF OUT	N/A	0X06 (6)	N/A	0x1E (SPDIF OUT)	N/A	0X16 (22,G)

CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER(INPUT)	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X15 (21,A)	VREF_A (50%)	0X15 (21,A)
SPDIF IN	N/A	0X0A (10)	0x1F (SPDIF IN)	N/A	N/A
MIC	0X24 (36)	0X07 (7)	0X19 (25,F)	VREF_F (100%)	N/A
HEADSET MIC	0X24 (36)	0X07 (7)	0X1B (27,E)	MIKEY	MIKEY



MagSafe DC Power Jack



DC-In & Battery Connectors

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

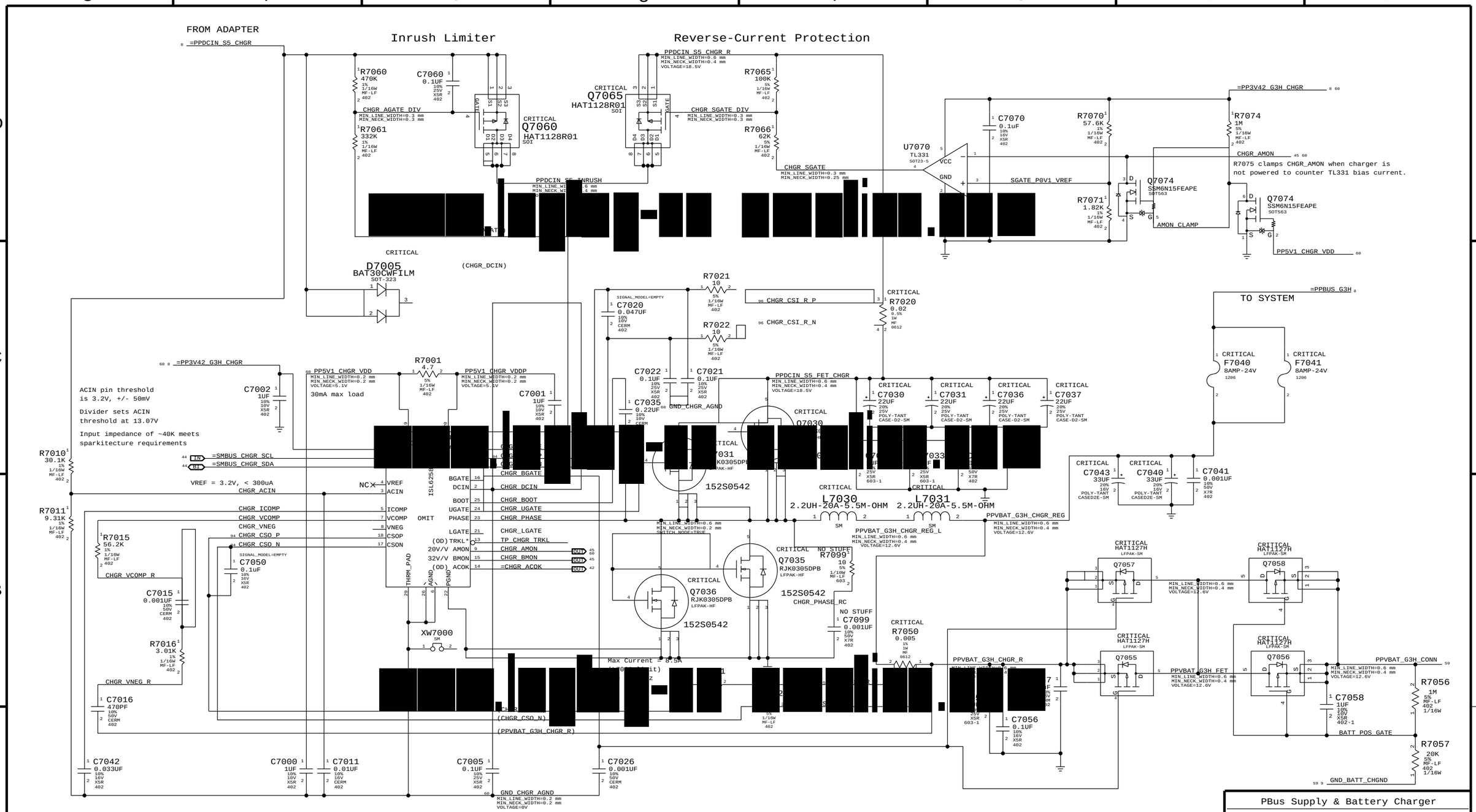
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

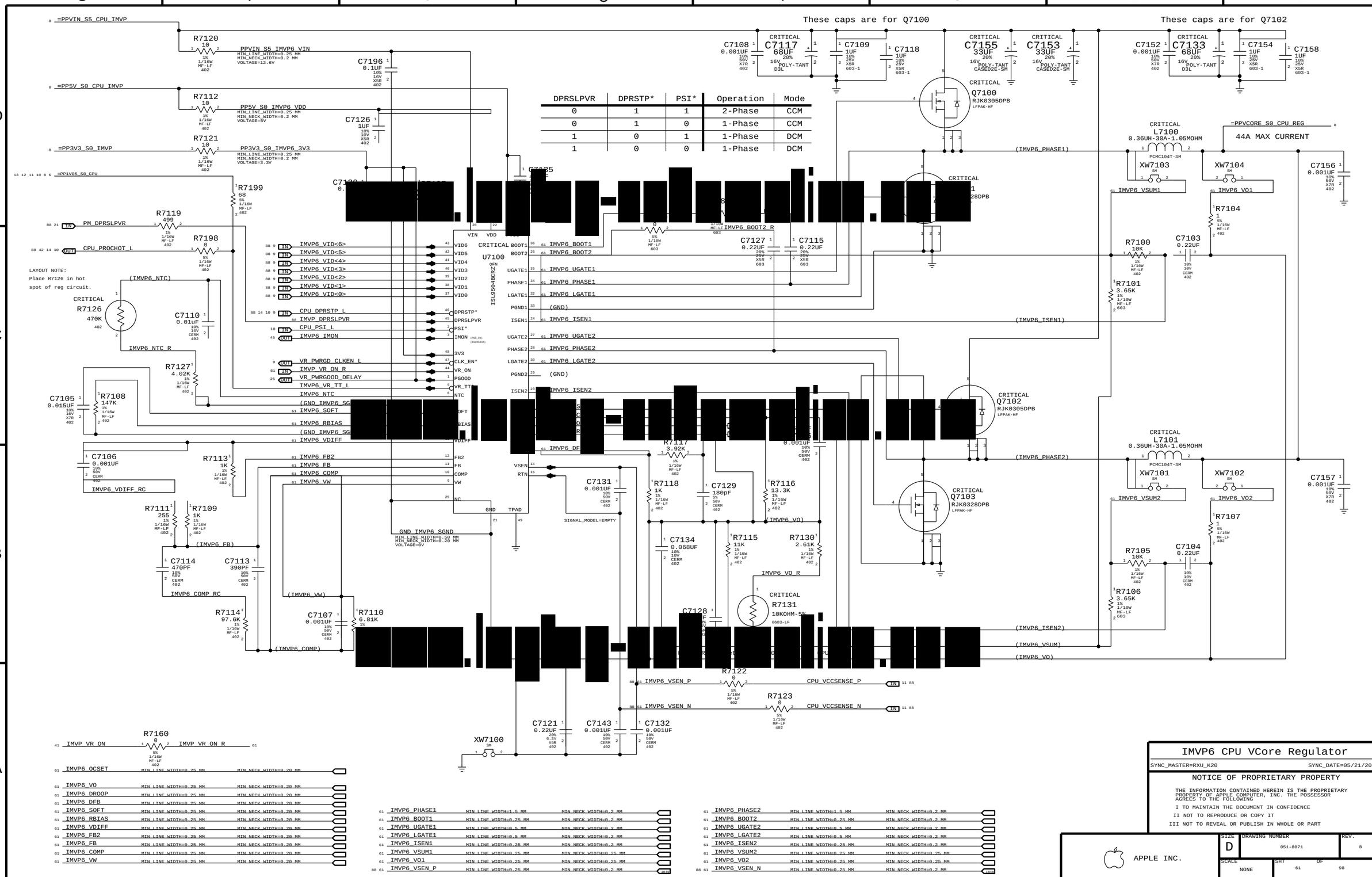
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 59 OF 98	



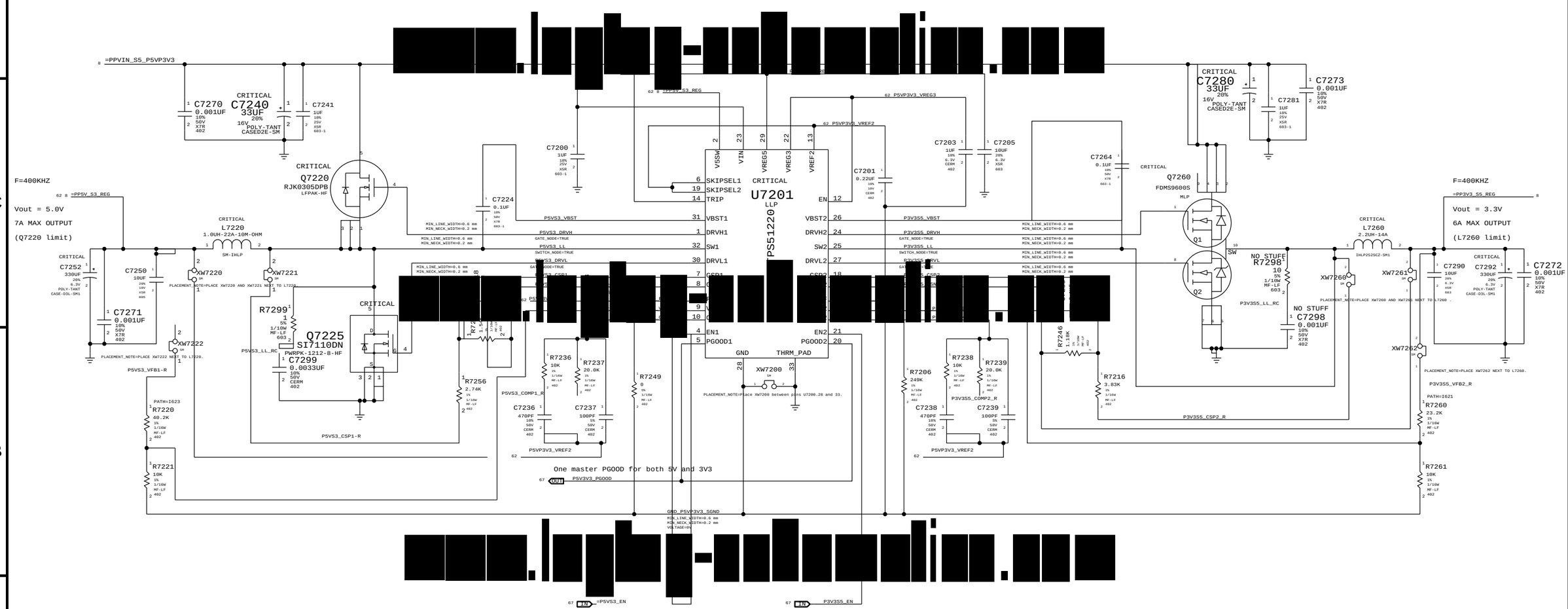
M99 differences from last sync on 12/02/07 to T18 MLB:

1. L7030 changed from T18 MLB inductor to 152S0542.
2. Added Q7056, C7058,R7055,R7056..
3. U7000 Thermal Pad is now connected to GND, not through XW.
4. Q7060 and Q7065 changed to 376S0667.
5. Q7055 and Q7056 changed to 376S0666.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
353S1938	1	IC,ISL6258,BAT CHARGER,28P,4X4,QFN,L	U7000	CRITICAL	ISL6258	2S Battery Default
353S1832	1	IC,ISL6258A,BAT CHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6258A	3S Battery Default



DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM



5V / 3.3V Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

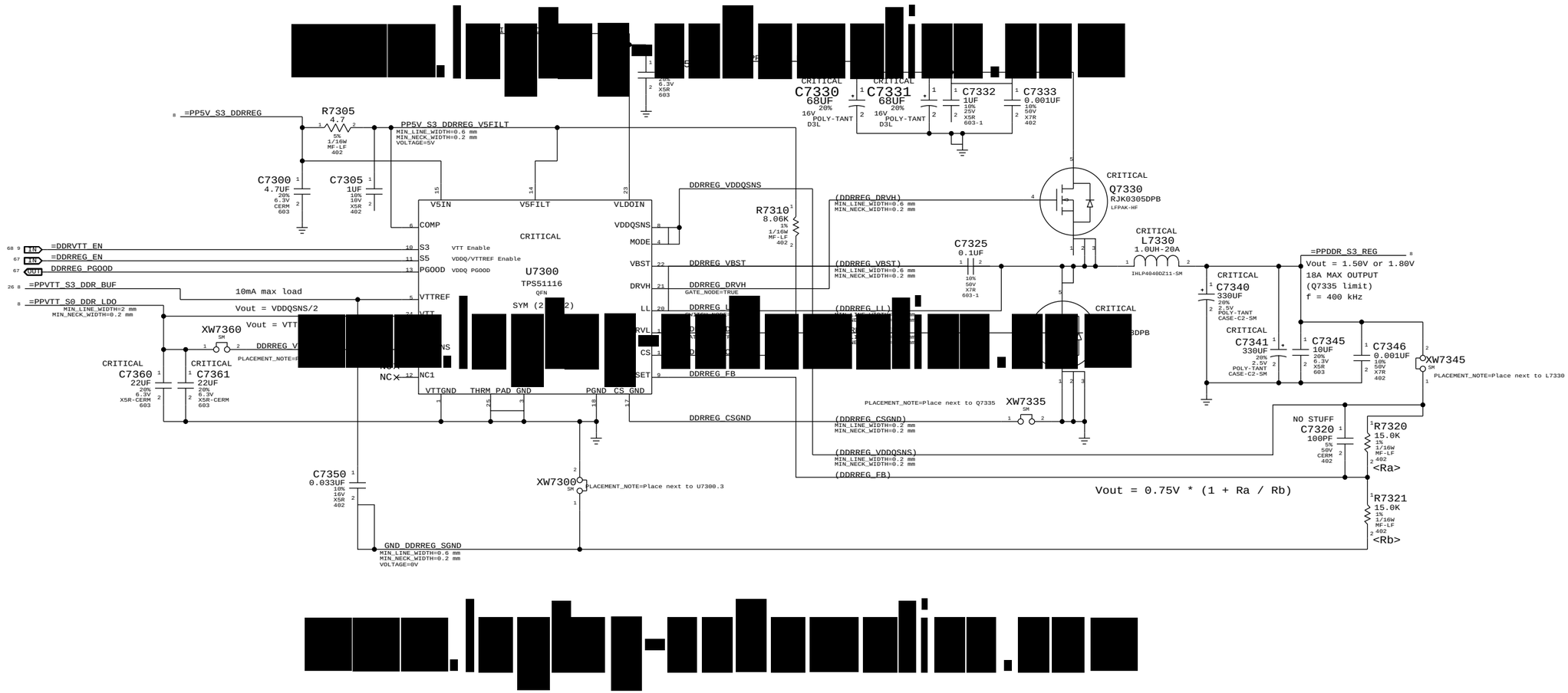
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 62	OF 98



1.5V DDR3 Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

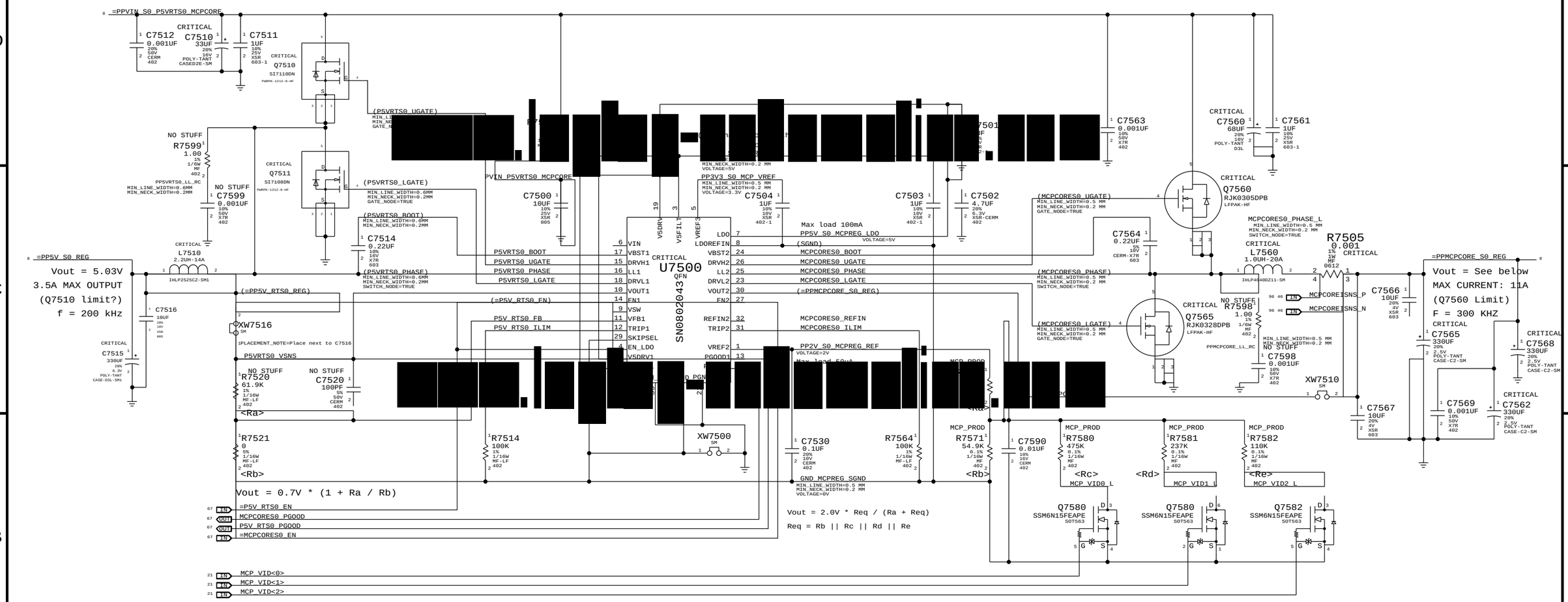
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 63 OF 98



MCP79 Rev A01 requires higher core & analog voltage

[redacted]

PART NUMBER	QTY	DESCRIPTION	REFERENCE D[redacted]CRITICAL [redacted]OM OPTION
114S0382	1	RES,MTL FILM,1/16W,48.7K,1,0402,SMD,LF	R7570	MCP_A01
114S0400	1	RES,MTL FILM,1/16W,76.8K,1,0402,SMD,LF	R7571	MCP_A01
114S0482	1	RES,MTL FILM,1/16W,523K,1,0402,SMD,LF	R7580	MCP_A01
114S0453	1	RES,MTL FILM,1/16W,267K,1,0402,SMD,LF	R7581	MCP_A01
114S0422	1	RES,MTL FILM,1/16W,130K,1,0402,SMD,LF	R7582	MCP_A01
114S0373	1	RES,MTL FILM,1/16W,40.2K,1,0402,SMD,LF	R7570	MCP_A01Q
114S0404	1	RES,MTL FILM,1/16W,84.5K,1,0402,SMD,LF	R7571	MCP_A01Q
114S0458	1	RES,MTL FILM,1/16W,301K,1,0402,SMD,LF	R7580	MCP_A01Q
114S0447	1	RES,MTL FILM,1/16W,237K,1,0402,SMD,LF	R7581	MCP_A01Q
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7582	MCP_A01Q

VID<2:0>	Rev A01 Voltage	Production Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

5V_S0 / MCP CORE REGULATOR

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

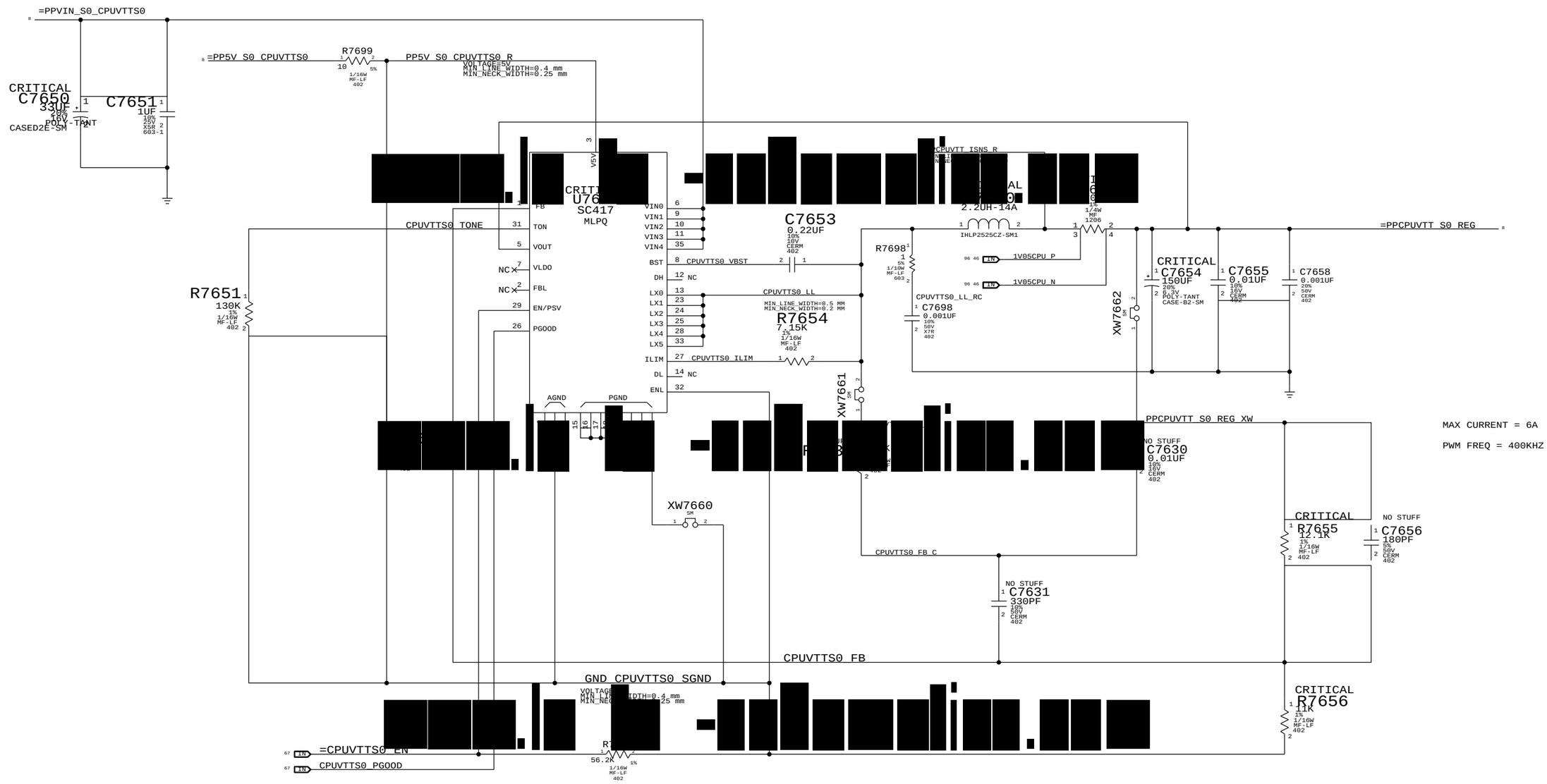
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 64 OF 98



CPU VTT Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

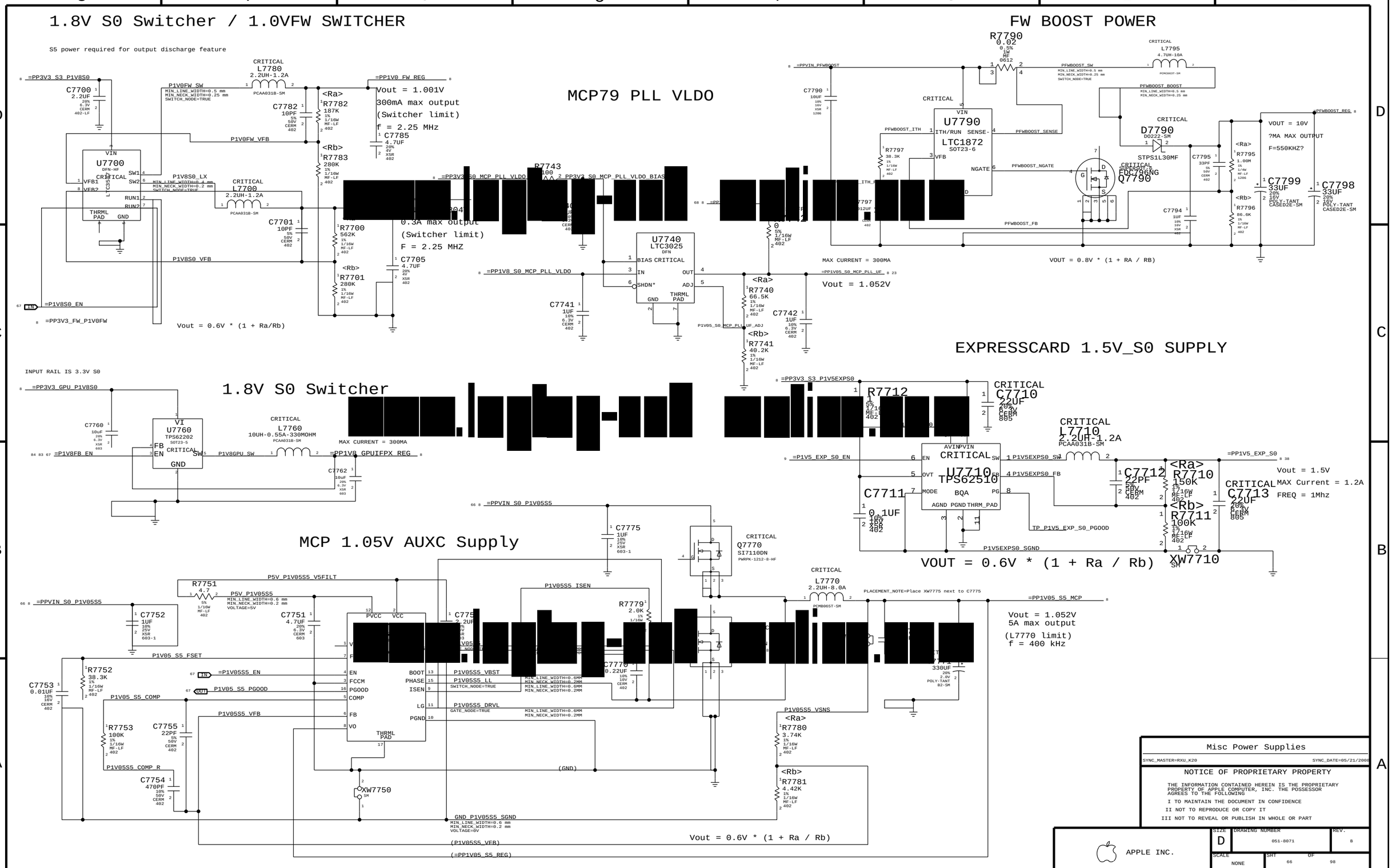
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

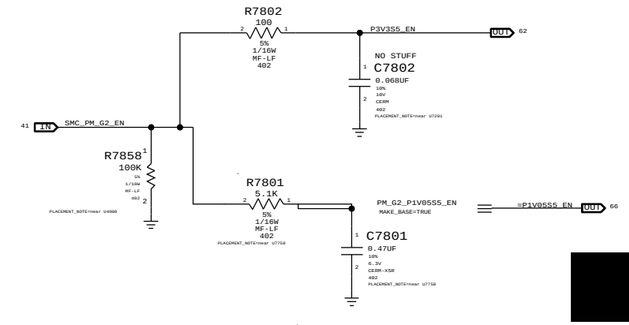
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 65 OF 98	

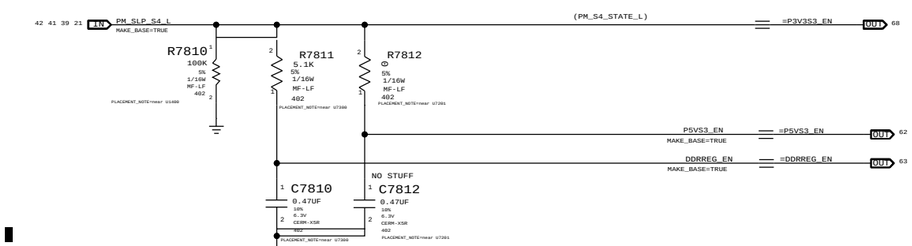

1.8V S0 Switcher / 1.0VFW SWITCHER
S5 power required for output discharge feature
=PP3V3_S3_P1V8S0
C7700 2.2UF
CRITICAL L7780 2.2UH-1.2A
P1V0FW_SW
=PP1V0_FW_REG
Vout = 1.001V
300mA max output
(Switcher limit)
f = 2.25 MHz
C7782 10PF
R7782 187K
C7785 4.7UF
P1V0FW_VFB
U7700
R7783 280K
P1V8S0_LX
CRITICAL L7700 2.2UH-1.2A
C7701 10PF
R7700 562K
0.3A max output
(Switcher limit)
F = 2.25 MHZ
C7705 4.7UF
R7701 280K
P1V8S0_VFB
=P1V8S0_EN
=PP3V3_FW_P1V0FW
Vout = 0.6V * (1 + Ra/Rb)
MCP79 PLL VLDO
R7743
=PP3V3_S0_MCP_PLL_VLDO
=PP3V3_S0_MCP_PLL_VLDO_BIAS
U7740 LTC3025
BIAS CRITICAL
=PP1V8_S0_MCP_PLL_VLDO
C7741 1UF
C7742 1UF
R7740 66.5K
R7741 40.2K
=PP1V05_S0_MCP_PLL_UF
Vout = 1.052V
MAX CURRENT = 300MA
FW BOOST POWER
R7790 0.02
=PPVIN_PFWBOOST
C7790 10UF
CRITICAL L7795 4.7UH-10A
PFWBOOST_SW
PFWBOOST_BOOST
U7790 LTC1872
PFWBOOST_ITH
PFWBOOST_SENSE
R7797 38.3K
NGATE
PFWBOOST_NGATE
PFWBOOST_FB
CRITICAL D7790 STPS1L30MF
CRITICAL FDC796NG Q7790
C7795 33PF
R7795 1.00M
R7796 86.6K
C7794 1UF
=PFWBOOST_REG
VOUT = 10V
?MA MAX OUTPUT
F=550KHZ?
C7799 33UF
C7798 33UF
VOUT = 0.8V * (1 + RA / RB)
EXPRESSCARD 1.5V_S0 SUPPLY
INPUT RAIL IS 3.3V S0
=PP3V3_GPU_P1V8S0
1.8V S0 Switcher
U7760 TPS62202
=P1V8FB_EN
CRITICAL L7760 10UH-0.55A-330MOHM
P1V8GPU_SW
=PP1V8_GPUIFPX_REG
MAX CURRENT = 300MA
=PP3V3_S3_P1V5EXPS0
R7712
CRITICAL C7710 22UF
CRITICAL L7710 2.2UH-1.2A
=PP1V5_EXP_S0
Vout = 1.5V
MAX Current = 1.2A
FREQ = 1Mhz
=PP1V5_EXP_S0_EN
U7710 TPS62510
C7711 0.1UF
C7712 22PF
R7710 150K
R7711 100K
CRITICAL C7713 22UF
XW7710
P1V5EXPS0_SGND
TP_P1V5_EXP_S0_PGOOD
VOUT = 0.6V * (1 + Ra / Rb)
MCP 1.05V AUXC Supply
=PPVIN_S0_P1V05S5
C7775 1UF
CRITICAL Q7770 SI7110DN
P5V_P1V05S5_V5FILT
R7751 4.7
C7752 1UF
C7751 4.7UF
P1V05S5_ISEN
R7779 2.0K
CRITICAL L7770 2.2UH-8.0A
PLACEMENT_NOTE=Place XW7775 next to C7775
=PP1V05_S5_MCP
Vout = 1.052V
5A max output
(L7770 limit)
f = 400 kHz
P1V05_S5_FSET
R7752 38.3K
C7753 0.01UF
=P1V05S5_EN
P1V05_S5_PGOOD
P1V05_S5_COMP
P1V05S5_VFB
R7753 100K
C7755 22PF
C7754 470PF
P1V05S5_VBST
P1V05S5_LL
P1V05S5_DRVL
C7770 0.22UF
330UF
P1V05S5_VSNS
R7780 3.74K
R7781 4.42K
XW7750
GND_P1V05S5_SGND
Vout = 0.6V * (1 + Ra / Rb)
(P1V05S5_VFB)
(=PP1V05_S5_REG)
Misc Power Supplies
SYNC_MASTER=RXU_K20
SYNC_DATE=05/21/2008
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE INC.
SIZE D
DRAWING NUMBER 051-8071
REV. 8
SCALE NONE
SHT 66 OF 98

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

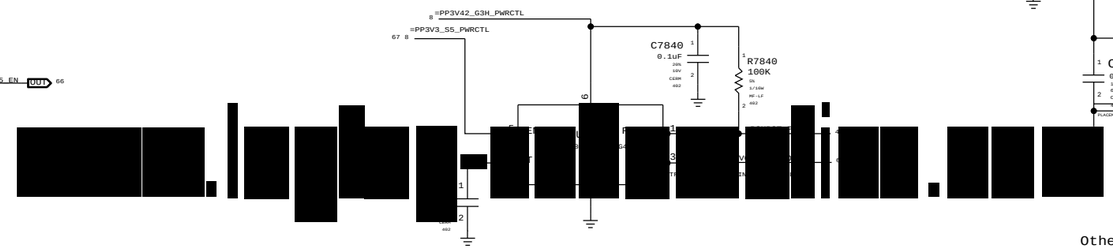
3.3V 1,05V S5 ENABLE



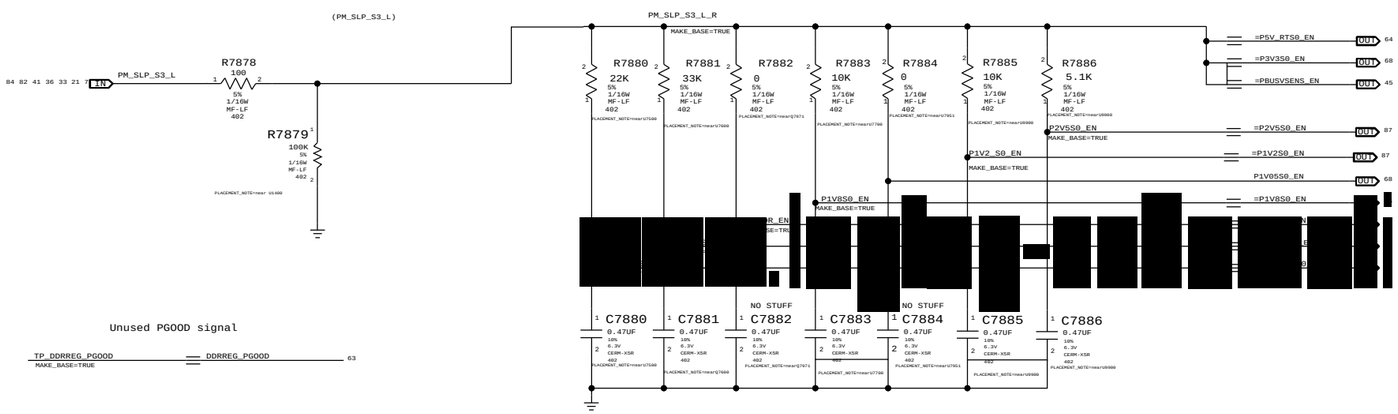
3.3V,5V S3 ENABLE



S5 rail PWRGD

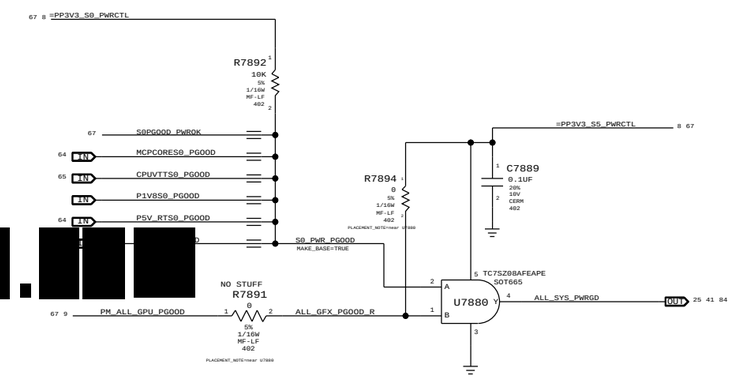


S0 ENABLE



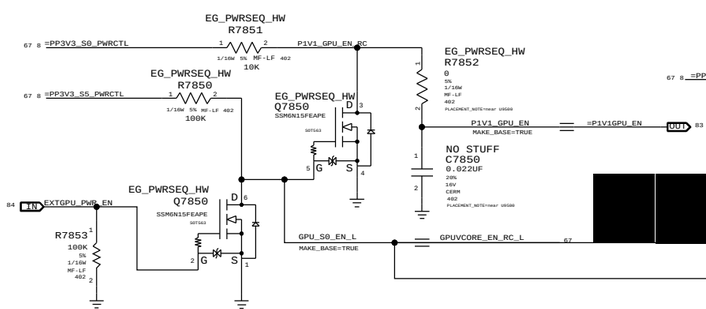
Other S0 RAILS

	PM_ALL_GFX_PGOOD
IG	high
EG	PM_ALL_GPU_PGOOD

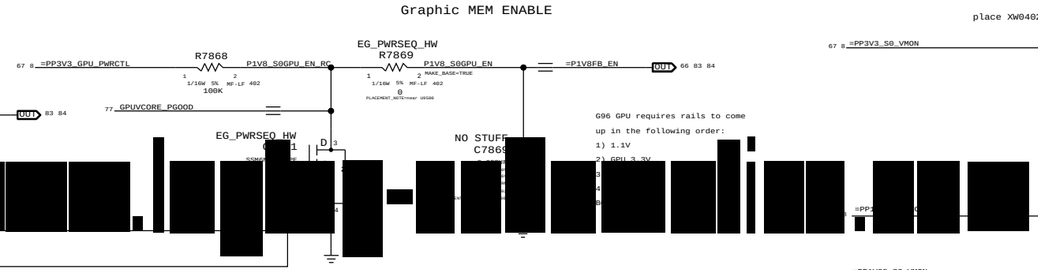


Unused PGOOD signal

1.1V GPU ENABLE

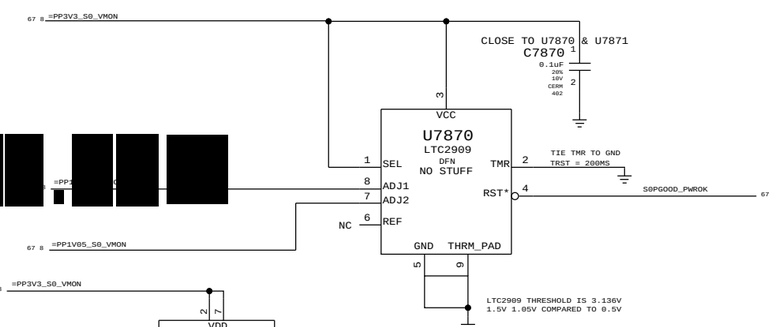


Graphic MEM ENABLE

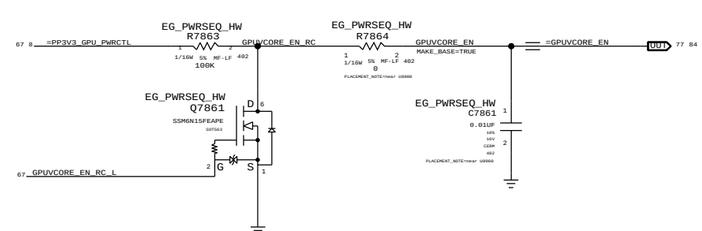


3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

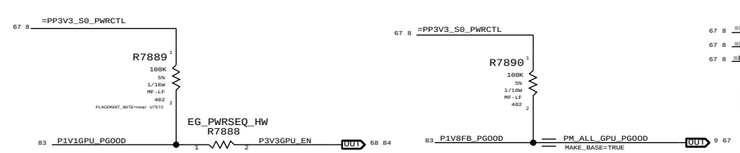
place XW0402 if needed to save trace space for pin 7,8



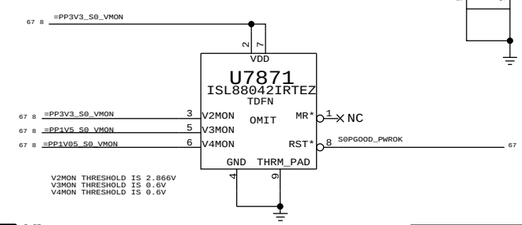
GPUVCORE ENABLE



EXT GPU PWRGD Pullup



U7871 IS TO REPLACE U7870



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2718	1	IC, QUAD VOLTAGE MONITOR	U7871	CRITICAL	

Power Control

SYNC_MASTER=YMA_K20 SYNC_DATE=09/09/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

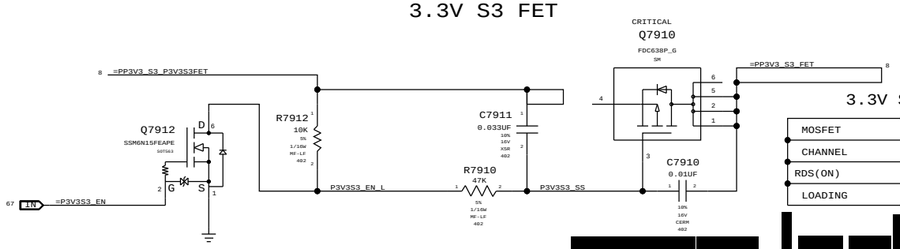
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 67 OF 98	

3.3V S3 FET

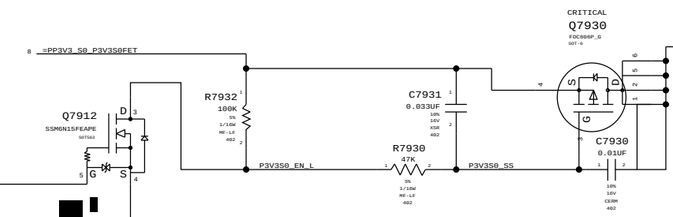


3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.087 A (EDP)

[redacted]

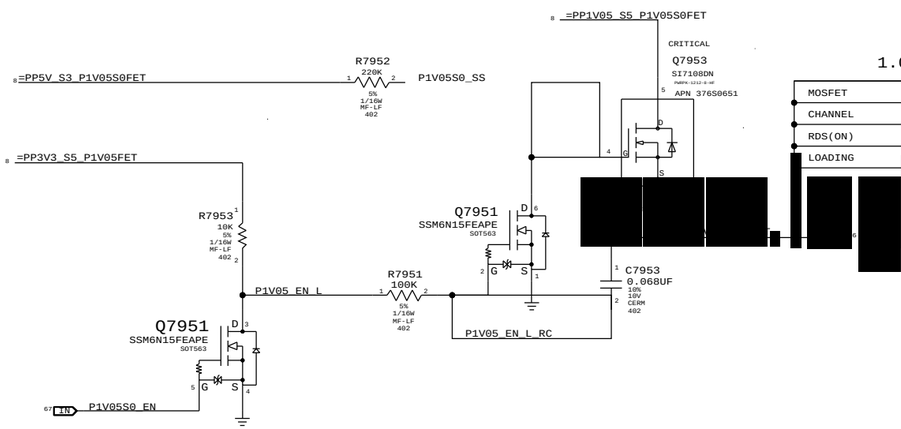
3.3V S0 FET



3.3V S0 FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	2.9 A (EDP)

1.05V S0 FET

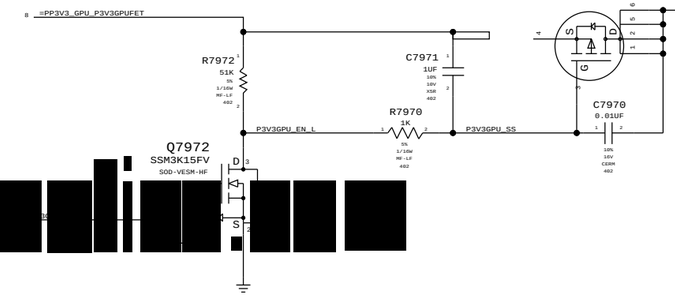


1.05V S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.1 A (EDP)

[redacted]

3.3V GPU FET



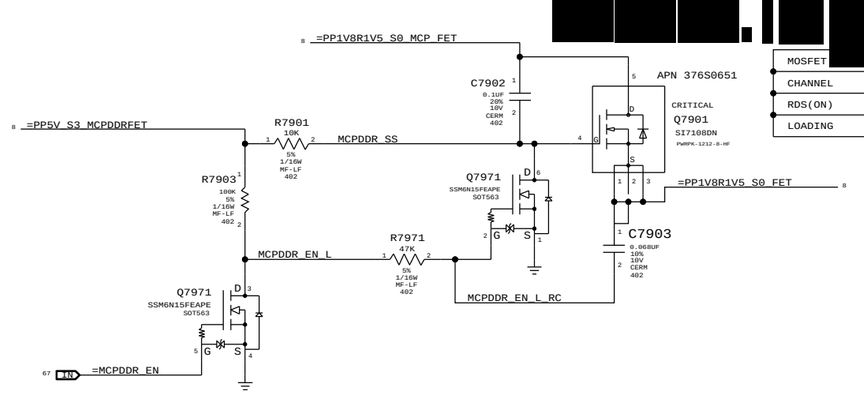
3.3V GPU FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	1.1 A (EDP)

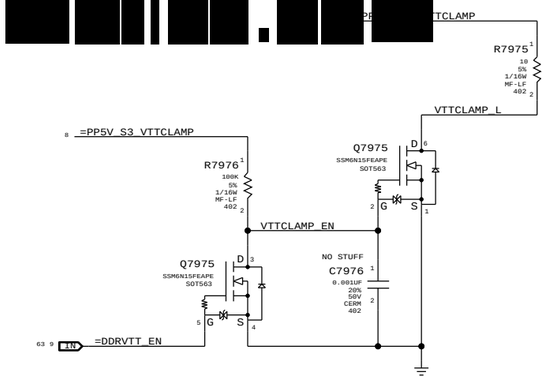
MCP79 DDR FETs

MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low before rail is turned off, and remains low until after rail turns back on or DIMMs will exit self-refresh prematurely. MEM_VTT_EN output from MCP79 used to enable clamp on VTT rail, which pulls all CKE signals low through VTT termination resistors.

1.5V S0 FET



[redacted]



Power FETs

SYNC_MASTER=YMA_K20 SYNC_DATE=05/19/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

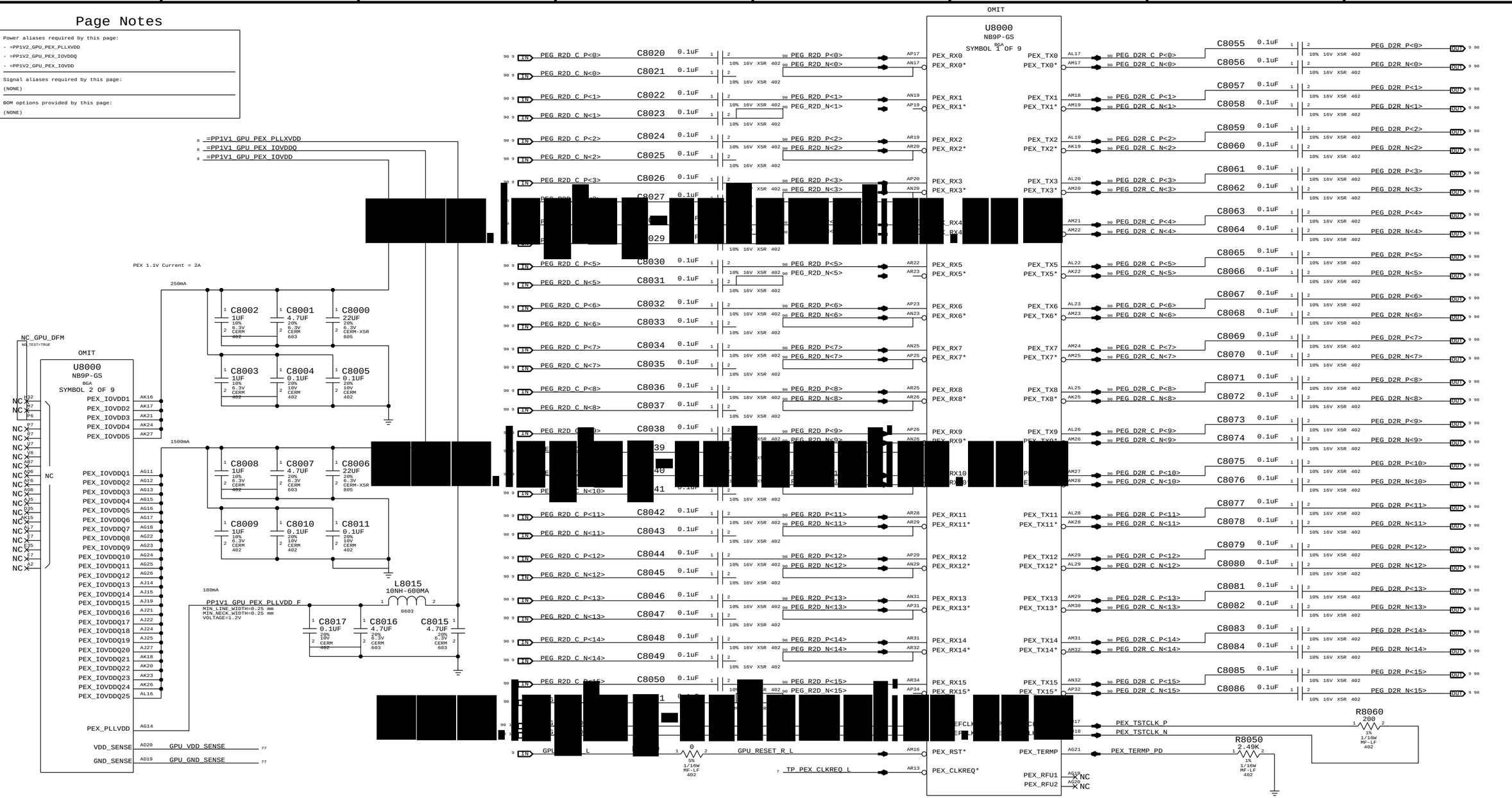
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 68	OF 98

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G96 PCI-E

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

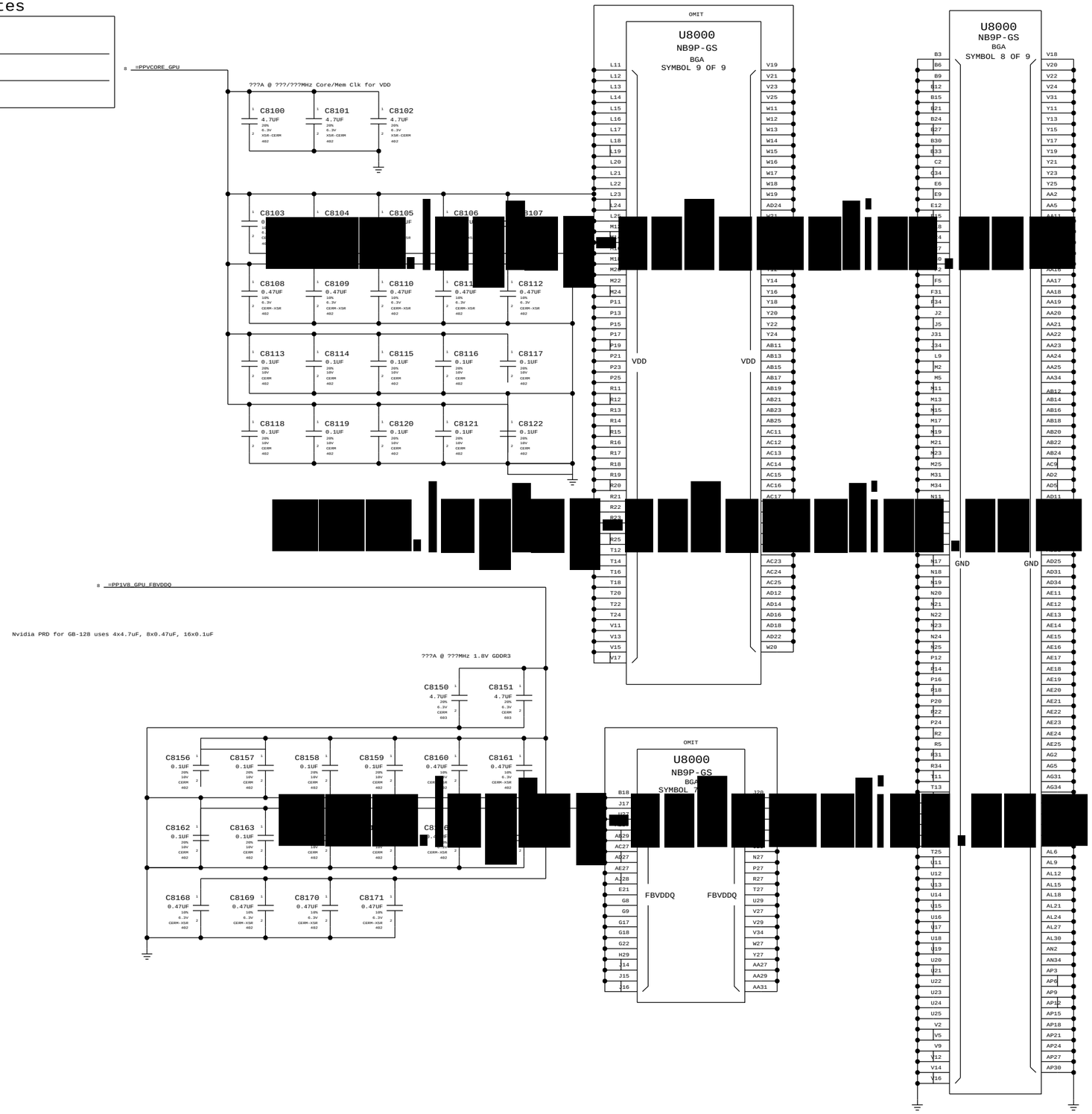
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 69 OF 98	

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G96 CORE/FB POWER

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

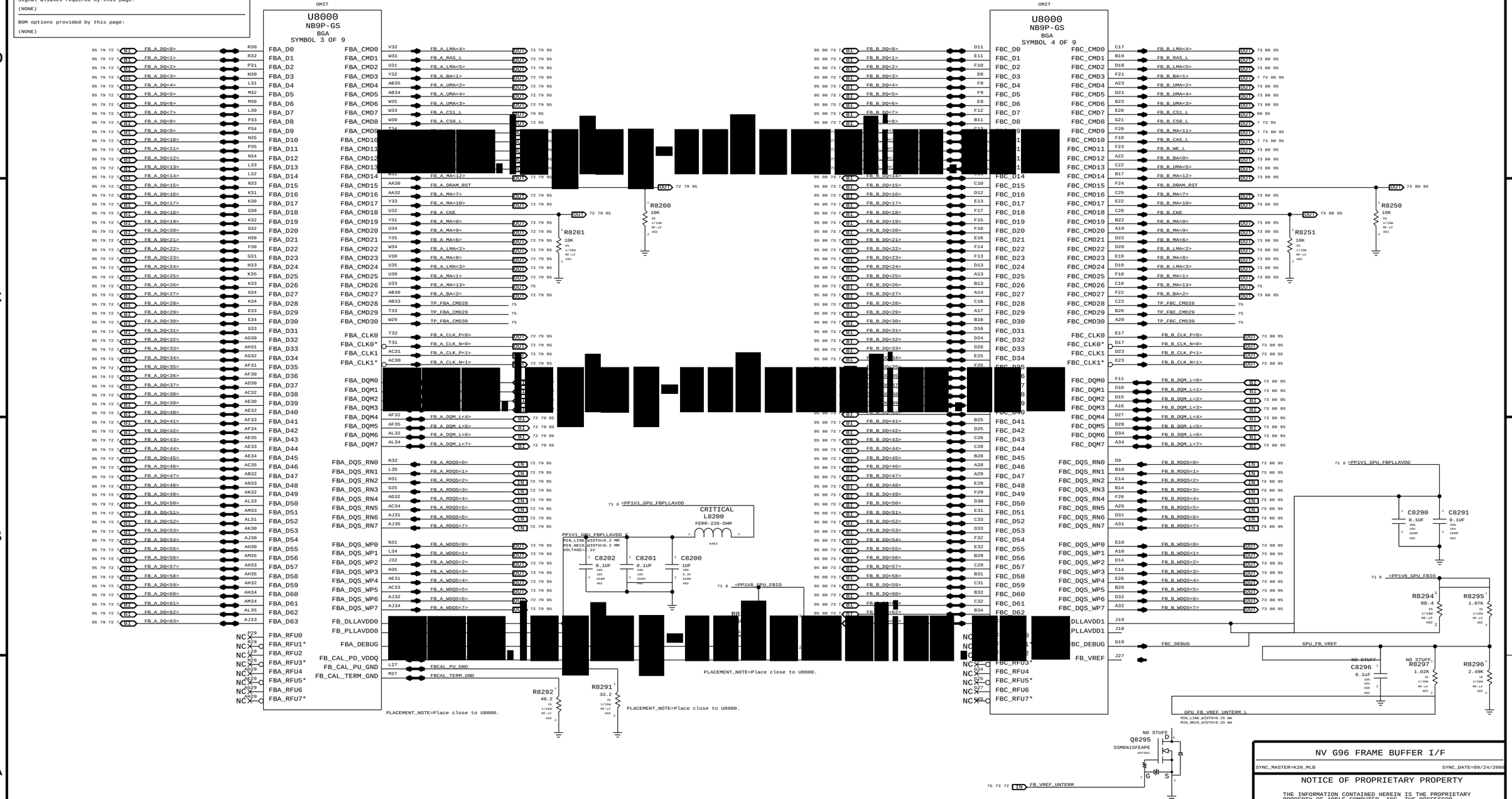
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 70 OF 98	

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G96 FRAME BUFFER I/F

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

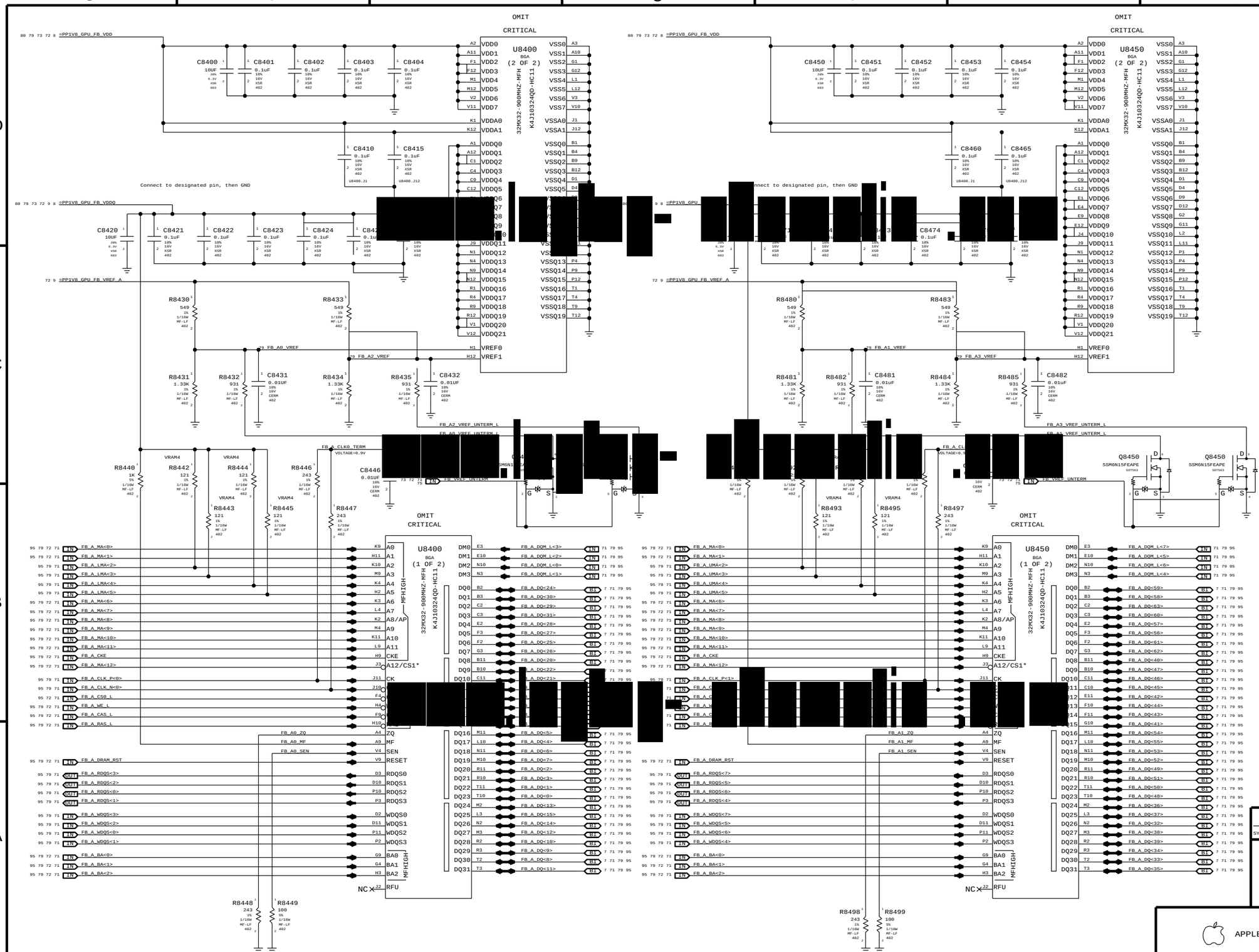
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 71 OF 98



Page Notes

Power aliases required by this page:

- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREFA

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

VRAM4

GDDR3 Frame Buffer A (Bottom)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

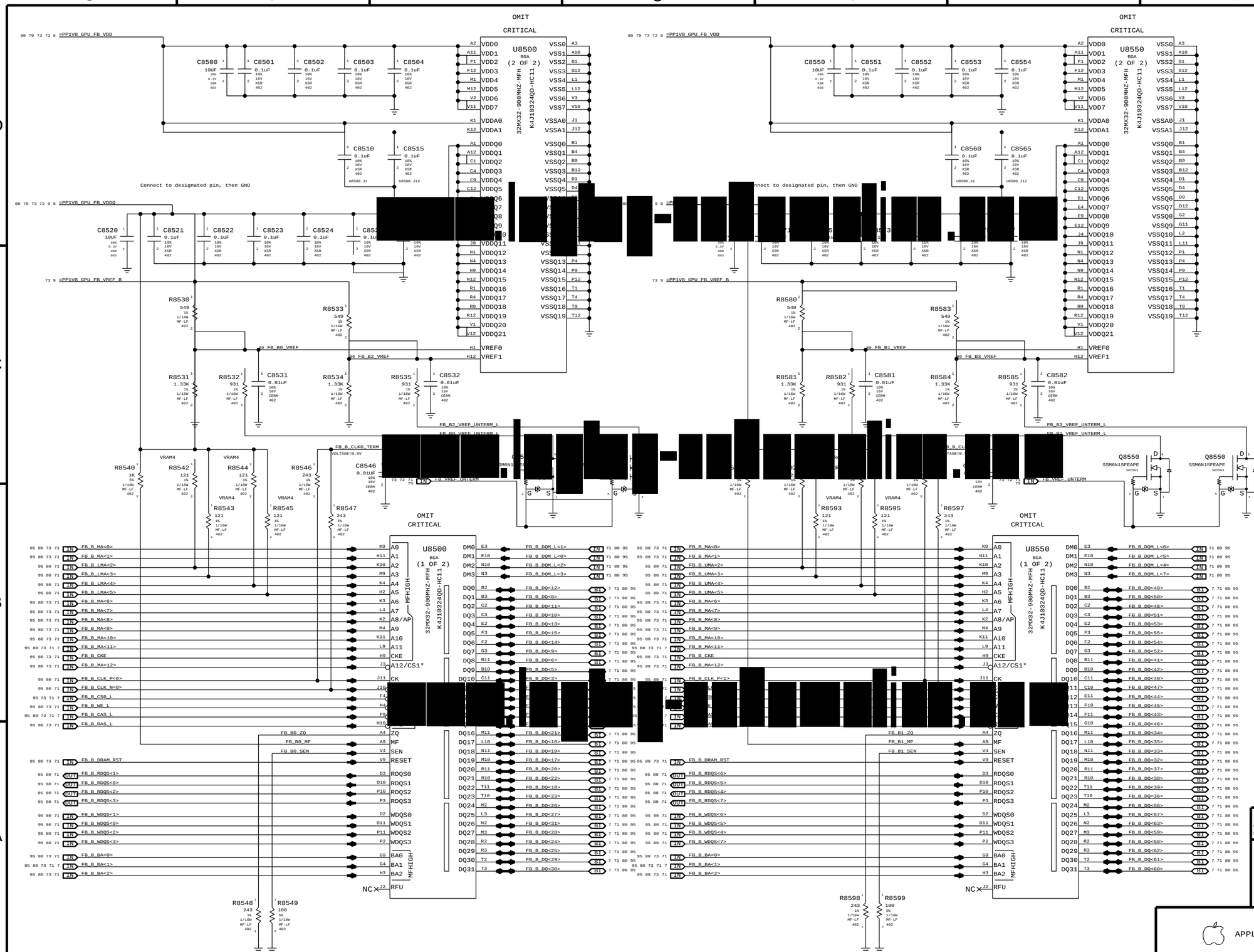
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 72 OF 98	



Page Notes

Power aliases required by this page:

- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREF_B

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

VRAM4

GDDR3 Frame Buffer B (Bottom)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

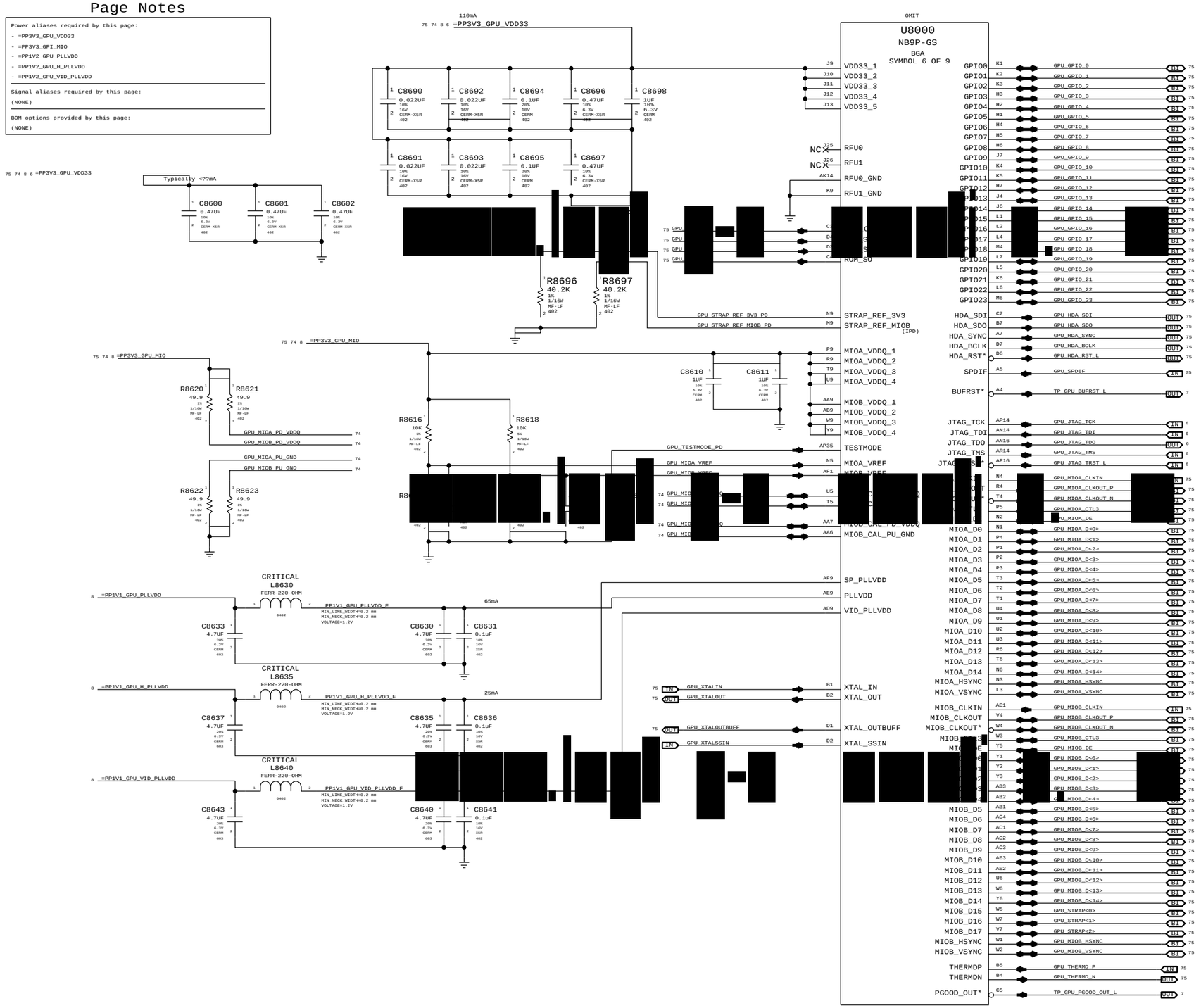
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 73	OF 98

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G96 GPIO/MIO/MISC

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 74	OF 98

GPIOs

	Native Func		
GPU_GPIO_0	GP	NC_GPU_GPIO_0	MAKE_BASE=TRUE, NO_TEST=TRUE
GPU_GPIO_1	HPDC	DP_EG_HPD	MAKE_BASE=TRUE
GPU_GPIO_2	LCD0_BL_PWM	TP_LVDS_EG_BKL_PWM	MAKE_BASE=TRUE
GPU_GPIO_3	LCD0_VDD	EG_LCD_PWR_EN	MAKE_BASE=TRUE
GPU_GPIO_4	LCD0_BL_EN	EG_BKLT_EN	MAKE_BASE=TRUE
GPU_GPIO_5	VID0	TP_GPU_GSTATE<0>	MAKE_BASE=TRUE
GPU_GPIO_6	VID1	TP_GPU_GSTATE<1>	MAKE_BASE=TRUE
GPU_GPIO_7	VID2/MEM_VID	GPIO7_FBVDD_ALTVO	MAKE_BASE=TRUE
GPU_GPIO_8	THERM	SMC_GFX_OVERTEMP_R_L	MAKE_BASE=TRUE
GPU_GPIO_9	FAN_PWM	SMC_GFX_THROTTLE_R_L	MAKE_BASE=TRUE
GPU_GPIO_10	MEM_VREF	FB_VREF_UNTERM	MAKE_BASE=TRUE
GPU_GPIO_11	SLI_SYNC	GPU_VCORE_VID0	MAKE_BASE=TRUE
GPU_GPIO_12	AC_DET	GPU_VCORE_VID1	MAKE_BASE=TRUE
GPU_GPIO_13	PWR_CTL0	GPU_VCORE_VID2	MAKE_BASE=TRUE
GPU_GPIO_14	PWR_CTL1	TP_GPU_VCORE_VID3	MAKE_BASE=TRUE

GPIOs

	Native Func		
GPU_GPIO_15	HPDE	NC_GPU_GPIO_15	MAKE_BASE=TRUE, NO_TEST=TRUE
GPU_GPIO_16	DVI_MODE0	EG_DP_CA_DET	
GPU_GPIO_17	HDMI_DETECT0	NC_GPU_GPIO_17	MAKE_BASE=TRUE, NO_TEST=TRUE
GPU_GPIO_18	DVI_MODE1	NC_GPU_GPIO_18	MAKE_BASE=TRUE, NO_TEST=TRUE
GPU_GPIO_19	HDMI_DETECT1	NC_GPU_GPIO_19	MAKE_BASE=TRUE, NO_TEST=TRUE
GPU_GPIO_20	HPDD	NC_GPU_GPIO_20	MAKE_BASE=TRUE, NO_TEST=TRUE
GPU_GPIO_21	HPDF	NC_GPU_GPIO_21	MAKE_BASE=TRUE, NO_TEST=TRUE
GPU_GPIO_22	SWAPRDY_A	NC_GPU_GPIO_22	MAKE_BASE=TRUE, NO_TEST=TRUE
GPU_GPIO_23	GP	NC_GPU_GPIO_23	MAKE_BASE=TRUE, NO_TEST=TRUE

Renamed signals

GPU_XTALOUT	GPU_XTALOUT	MAKE_BASE=TRUE
GPU_CLK27M	GPU_XTALIN	MAKE_BASE=TRUE
GPU_CLK27M_SS	GPU_XTALSSIN	MAKE_BASE=TRUE
GPU_TDIODE_P	GPU_THERMD_P	MAKE_BASE=TRUE
GPU_TDIODE_N	GPU_THERMD_N	MAKE_BASE=TRUE
LVDS_EG_DDC_CLK	GPU_I2CA_SCL	MAKE_BASE=TRUE
LVDS_EG_DDC_DATA	GPU_I2CA_SDA	MAKE_BASE=TRUE
DP_EG_DDC_CLK	GPU_I2CB_SCL	MAKE_BASE=TRUE
DP_EG_DDC_DATA	GPU_I2CB_SDA	MAKE_BASE=TRUE

Unused signals

NC_GPU_SPDIF	GPU_SPDIF	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_CPU_HDA_SDI	GPU_HDA_SDI	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_CPU_HDA_SDO	GPU_HDA_SDO	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_CPU_HDA_SYNC	GPU_HDA_SYNC	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_CPU_HDA_BCLK	GPU_HDA_BCLK	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_CPU_HDA_RST_L	GPU_HDA_RST_L	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_FBA_MA<13>	FB_A_MA<13>	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_FBB_MA<13>	FB_B_MA<13>	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_FBA_CMD28	TP_FBA_CMD28	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_FBC_CMD28	TP_FBC_CMD28	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_FBA_CMD29	TP_FBA_CMD29	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_FBC_CMD29	TP_FBC_CMD29	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_FBA_CMD30	TP_FBA_CMD30	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_FBC_CMD30	TP_FBC_CMD30	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_ROM_CS_L	GPU_ROM_CS_L	MAKE_BASE=TRUE, NO_TEST=TRUE

[redacted]

Unused I2C Buses

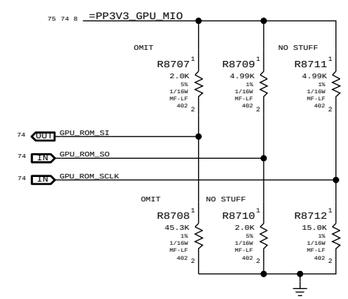
[redacted]	[redacted]	NO_TEST=TRUE
[redacted]	[redacted]	NO_TEST=TRUE
[redacted]	[redacted]	NO_TEST=TRUE
[redacted]	[redacted]	NO_TEST=TRUE
NC_GPU_I2CE_SCL	GPU_I2CE_SCL	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_I2CE_SDA	GPU_I2CE_SDA	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_I2CH_SCL	GPU_I2CH_SCL	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_I2CH_SDA	GPU_I2CH_SDA	MAKE_BASE=TRUE, NO_TEST=TRUE

I2CS ties into SMBus connection page

(I2CS requires pullups even if not used)

TP_LVDS_EG_B_CLK_P	LVDS_EG_B_CLK_P	MAKE_BASE=TRUE
TP_LVDS_EG_B_CLK_N	LVDS_EG_B_CLK_N	MAKE_BASE=TRUE
NC_LVDS_EG_A_DATA_P<3>	LVDS_EG_A_DATA_P<3>	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_LVDS_EG_A_DATA_N<3>	LVDS_EG_A_DATA_N<3>	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_LVDS_EG_B_DATA_P<3>	LVDS_EG_B_DATA_P<3>	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_LVDS_EG_B_DATA_N<3>	LVDS_EG_B_DATA_N<3>	MAKE_BASE=TRUE, NO_TEST=TRUE

Config Straps



Physical Strapping Pin	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM100
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

Strap S1/S2 Bit[3:0] PU/PD Rval

0 0000 PD 5k
1 0001 PD 10k
2 0010 PD 15k
3 0011 PD 20k
4 0100 PD 25k
5 0101 PD 30k
6 0110 PD 35k
7 0111 PD 45k

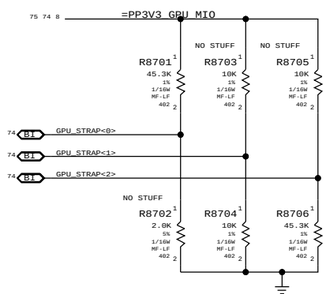
Strap S1/S2 Bit[3:0] PU/PD Rval

8 1000 PU 5k
9 1001 PU 10k
A 1010
B 1011
C 1100
D 1101
E 1110
F 1111 PU 45k

[redacted]

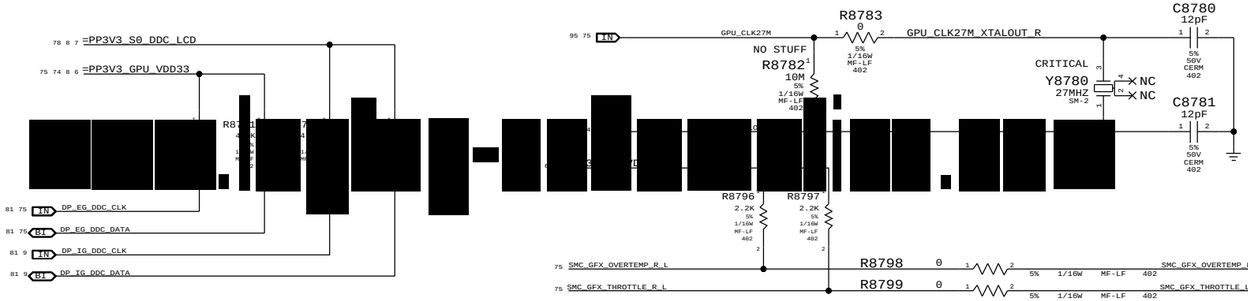
G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.

NC_GPU_MIOA_CLKOUT_P	GPU_MIOA_CLKOUT_P	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_MIOA_CLKOUT_N	GPU_MIOA_CLKOUT_N	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_MIOA_CTL3	GPU_MIOA_CTL3	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_GPU_MIOA_DE	GPU_MIOA_DE	MAKE_BASE=TRUE
TP_GPU_MIOA_D<9..0>	GPU_MIOA_D<9..0>	MAKE_BASE=TRUE
NC_GPU_MIOA_CLKIN	GPU_MIOA_CLKIN	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_MIOA_D<14..10>	GPU_MIOA_D<14..10>	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_MIOA_HSYNC	GPU_MIOA_HSYNC	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_MIOA_VSYNC	GPU_MIOA_VSYNC	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_MIOB_CLKIN	GPU_MIOB_CLKIN	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_MIOB_CLKOUT_P	GPU_MIOB_CLKOUT_P	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_MIOB_CLKOUT_N	GPU_MIOB_CLKOUT_N	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_MIOB_CTL3	GPU_MIOB_CTL3	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_MIOB_DE	GPU_MIOB_DE	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_MIOB_D<14..0>	GPU_MIOB_D<14..0>	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_MIOB_VSYNC	GPU_MIOB_VSYNC	MAKE_BASE=TRUE, NO_TEST=TRUE
NC_GPU_MIOB_HSYNC	GPU_MIOB_HSYNC	MAKE_BASE=TRUE, NO_TEST=TRUE

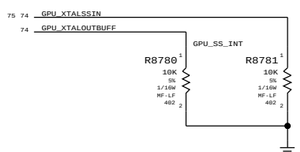


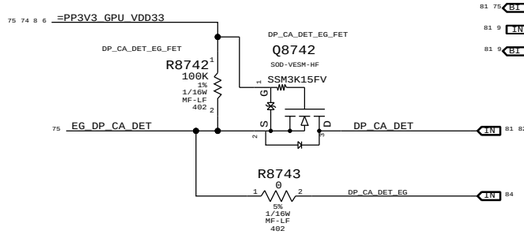
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0378	1	RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0378	1	RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF	R8707		VRAM_1024_SAMSUNG
114S0368	1	RES,MTL FILM,1/16W,35.7K,1,0402,SMD,LF	R8708		VRAM_512_HYNIX

GPU 27MHz Crystal

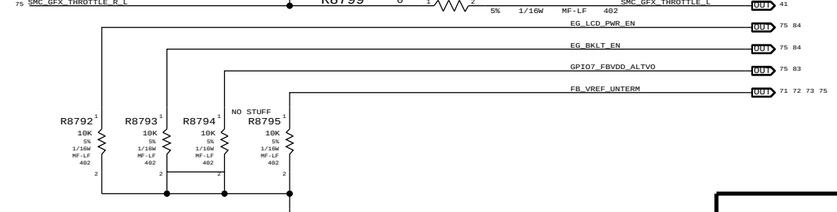


Unused Clocks





Isolation FETs for DP MUX inputs



G96 GPIOs & Straps

SYNC_MASTER=M98_MLB SYNC_DATE=05/12/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 75 OF 98	

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

=PP1V8_GPU_IFPX

CRITICAL
L8800
FERR-220-OHM
0402

?mA peak per diff pair
?mA peak for all pairs

C8800 4.7UF 20% 6.3V CERM 603 — Place at AG9
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402 — Place at AG10

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

GPU_IFPEF_RSET 76
GPU_IFPCD_RSET 76
GPU_IFPAB_RSET 76

R8855 1K 1% 1/16W MF-LF 402
R8850 1K 1% 1/16W MF-LF 402
R8851 1K 1% 1/16W MF-LF 402

CRITICAL
L8805
FERR-220-OHM
0402

80mA peak

C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

=PP1V1_GPU_IFPCD_IOVDD

CRITICAL
L8810
FERR-220-OHM
0402

?mA peak per diff pair
?mA peak for all pairs

C8810 4.7UF 20% 6.3V CERM 603 — Place at AJ8
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402 — Place at AK8

PP1V1_GPU_IFPCD_IOVDD_F 76
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

CRITICAL
L8815
FERR-220-OHM
0402

160mA peak

C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPCD_PLLVDD_F 76
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

I2CS must be pulled up if not used.
I2CS addr fixed a[redacted]0x9F

PP1V1_GPU_IFPEF_IOVDD_F 76
PP1V8_GPU_IFPEF_PLLVDD_F 76

Power inputs must be pulled down if not used

R8856 10K 5% 1/16W MF-LF 402
R8857 10K 5% 1/16W MF-LF 402

OMIT

U8000
NB9P-GS
BGA
SYMBOL 5 OF 9

76 PP1V1_GPU_IFPCD_IOVDD_F — AG9 IFPA_IOVDD, AG10 IFPB_IOVDD, AJ8 IFPC_IOVDD, AK8 IFPD_IOVDD
76 PP1V1_GPU_IFPEF_IOVDD_F — AE7 IFPE_IOVDD, AD7 IFPF_IOVDD
76 GPU_IFPAB_RSET — AK9 IFPAB_PLLVDD, AJ11 IFPAB_RSET

[redacted]

76 B1 GPU_I2CA_SCL	G1	I2CA_SCL	
76 B1 GPU_I2CA_SDA	G4	I2CA_SDA	
76 B1 GPU_I2CC_SCL	E3	I2CC_SCL	
76 B1 GPU_I2CC_SDA	E4	I2CC_SDA	
44 B1 =GPU_I2CS_SCL	E2	I2CS_SCL	
44 B1 =GPU_I2CS_SDA	E1	I2CS_SDA	
76 B1 GPU_I2CB_SCL	G3	I2CB_SCL	
76 B1 GPU_I2CB_SDA	G2	I2CB_SDA	
76 B1 GPU_I2CD_SCL	F4	I2CD_SCL	
76 B1 GPU_I2CD_SDA	G5	I2CD_SDA	
76 B1 GPU_I2CE_SCL	D5	I2CE_SCL	
76 B1 GPU_I2CE_SDA	E5	I2CE_SDA	

AM11	IFPA_TXC	LVDS_EG_A_CLK_P	OUT 84 95
AM12	IFPA_TXC*	LVDS_EG_A_CLK_N	OUT 84 95
AM8	IFPA_TXD0	LVDS_EG_A_DATA_P<0>	OUT 84 95
AL8	IFPA_TXD0*	LVDS_EG_A_DATA_N<0>	OUT 84 95
AM10	IFPA_TXD1	LVDS_EG_A_DATA_P<1>	OUT 84 95
AM9	IFPA_TXD1*	LVDS_EG_A_DATA_N<1>	OUT 84 95
AK10	IFPA_TXD2	LVDS_EG_A_DATA_P<2>	OUT 84 95
AL10	IFPA_TXD2*	LVDS_EG_A_DATA_N<2>	OUT 7 84 95
		LVDS_EG_A_DATA_P<3>	OUT 75
		LVDS_EG_A_DATA_N<3>	OUT 75
		LVDS_EG_B_CLK_P	OUT 75
		LVDS_EG_B_CLK_N	OUT 75
AN8	IFPB_TXD4	LVDS_EG_B_DATA_P<0>	OUT 84 95
AP8	IFPB_TXD4*	LVDS_EG_B_DATA_N<0>	OUT 84 95
AP10	IFPB_TXD5	LVDS_EG_B_DATA_P<1>	OUT 84 95
AN10	IFPB_TXD5*	LVDS_EG_B_DATA_N<1>	OUT 84 95
AR11	IFPB_TXD6	LVDS_EG_B_DATA_P<2>	OUT 84 95
AR10	IFPB_TXD6*	LVDS_EG_B_DATA_N<2>	OUT 84 95
AN11	IFPB_TXD7	LVDS_EG_B_DATA_P<3>	OUT 75
AP11	IFPB_TXD7*	LVDS_EG_B_DATA_N<3>	OUT 75
AP2	IFPC_AUX	DP_EG_AUX_CH_P	OUT 81 95
AN3	IFPC_AUX*	DP_EG_AUX_CH_N	OUT 81 95
AM7	IFPC_L0	DP_EG_ML_P<0>	OUT 81 95
AM6	IFPC_L0*	DP_EG_ML_N<0>	OUT 81 95
AL5	IFPC_L1	DP_EG_ML_P<1>	OUT 81 95
AM5	IFPC_L1*	DP_EG_ML_N<1>	OUT 81 95
AM3	IFPC_L2	DP_EG_ML_P<2>	OUT 81 95
AM4	IFPC_L2*	DP_EG_ML_N<2>	OUT 81 95
AP1	IFPC_L3	DP_EG_ML_P<3>	OUT 81 95
AR2	IFPC_L3*	DP_EG_ML_N<3>	OUT 81 95
AP4	IFPD_AUX		NC
AN4	IFPD_AUX*		NC
AN6	IFPD_L2		NC
AP6	IFPD_L2*		NC
AP5	IFPD_L3		NC
AN5	IFPD_L3*		NC
AE4	IFPE_AUX		NC
AD4	IFPE_AUX*		NC
AH6	IFPE_L0		NC
AH5	IFPE_L0*		NC
AH4	IFPE_L1		NC
AG4	IFPE_L1*		NC
AE5	IFPE_L2		NC
AE6	IFPE_L2*		NC
AE3	IFPE_L3		NC
AE2	IFPE_L3*		NC
AF3	IFPF_AUX		NC
AF2	IFPF_AUX*		NC
AL2	IFPF_L0		NC
AL1	IFPF_L0*		NC
AJ3	IFPF_L1		NC
AJ2	IFPF_L1*		NC

R8861 1K 5% 1/16W MF-LF 402
NO STUFF
R8860 1K 5% 1/16W MF-LF 402

[redacted]

AJ12	DACA_VDD	DACA_RED	AM15 NC
		DACA_GREEN	AM14 NC
		DACA_BLUE	AL14 NC
NC AK12	DACA_VREF	DACA_HSYNC	AM13 NC
NC AK13	DACA_RSET	DACA_VSYNC	AL13 NC
AC6	DACB_VDD	DACB_RED	AA4 NC
		DACB_GREEN	AB4 NC
		DACB_BLUE	Y4 NC
NC AC5	DACB_VREF	DACB_CSYNC	AB5 NC
NC AB6	DACB_RSET		
AG7	DACC_VDD	DACC_RED	AK4 NC
		DACC_GREEN	AL4 NC
		DACC_BLUE	AJ4 NC
NC AK6	DACC_VREF	DACC_HSYNC	AN2 NC
NC AG7	DACC_RSET	DACC_VSYNC	AK2 NC

GPU_DACA_VDD
GPU_DACB_VDD
GPU_DACC_VDD

R8852 10K 5% 1/16W MF-LF 402
R8853 10K 5% 1/16W MF-LF 402
R8854 10K 5% 1/16W MF-LF 402

NV G96 Video Interfaces

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

NOTICE OF PROPRIETARY PROPERTY

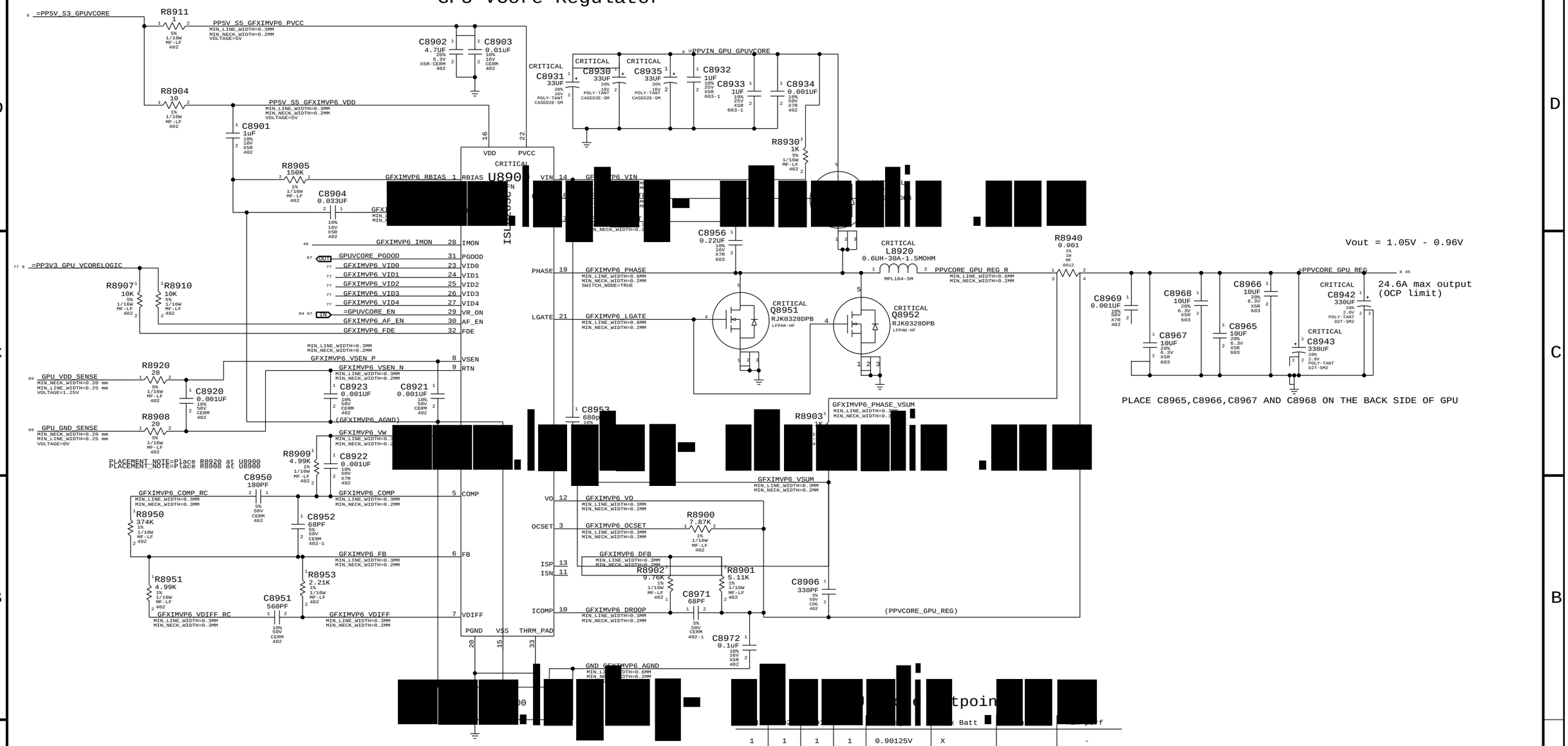
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 76 OF 98	

GPU VCore Regulator

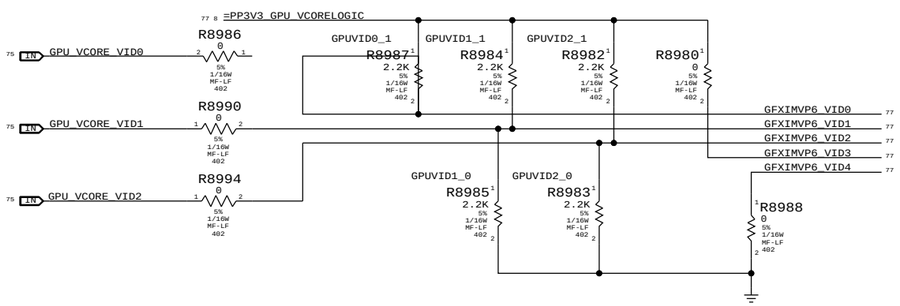


[redacted]

[redacted]

1	1	1	1	0.90125V	X		-
1	1	1	0	0.92700V	-	X	-
1	1	0	1	1.00425V	-	-	X

Other VID states may not be valid



Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P90V	GPUVID2_1,GPUVID1_1,GPUVID0_1
GPUVID_1P00V	GPUVID2_0,GPUVID1_1,GPUVID0_1

GPU (G96) CORE SUPPLY

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

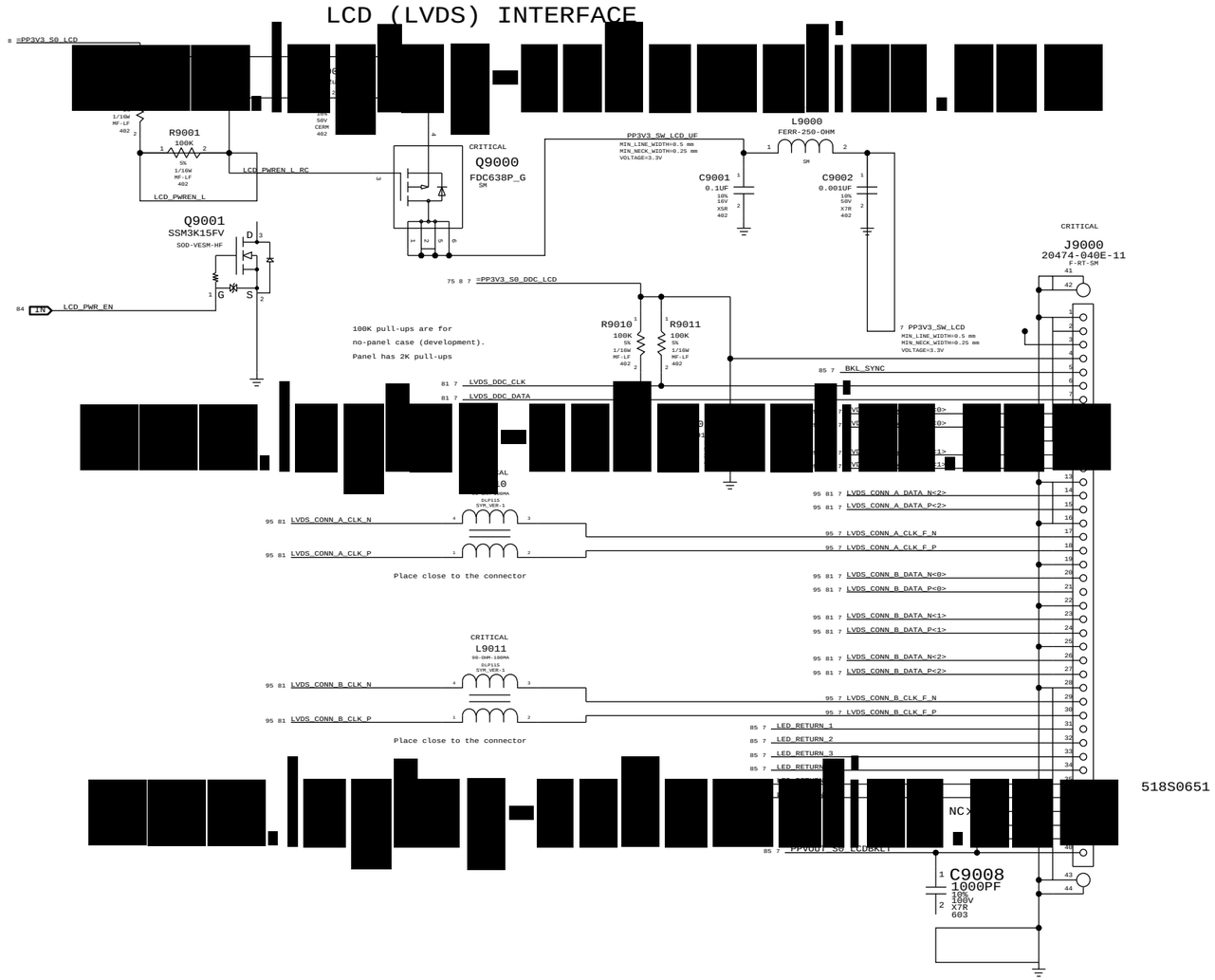
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 77 OF 98	

LCD (LVDS) INTERFACE



518S0651

LVDS Display Connector

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

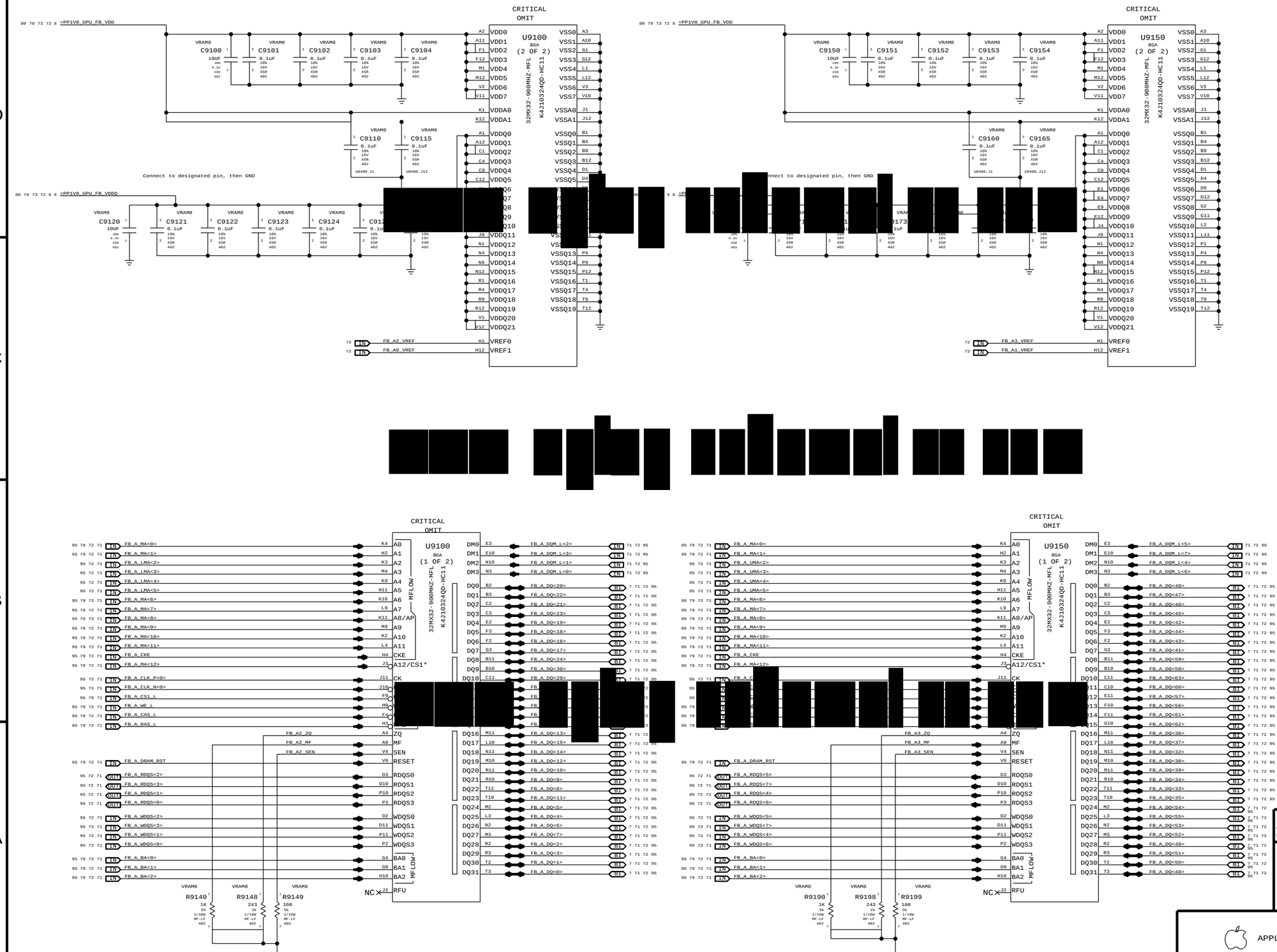
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 78 OF 98	



Page Notes

Power aliases required by this page:

- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

VRAM8

GDDR3 Frame Buffer A (Top)

SYNC_MASTER=M99_MLB SYNC_DATE=04/04/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

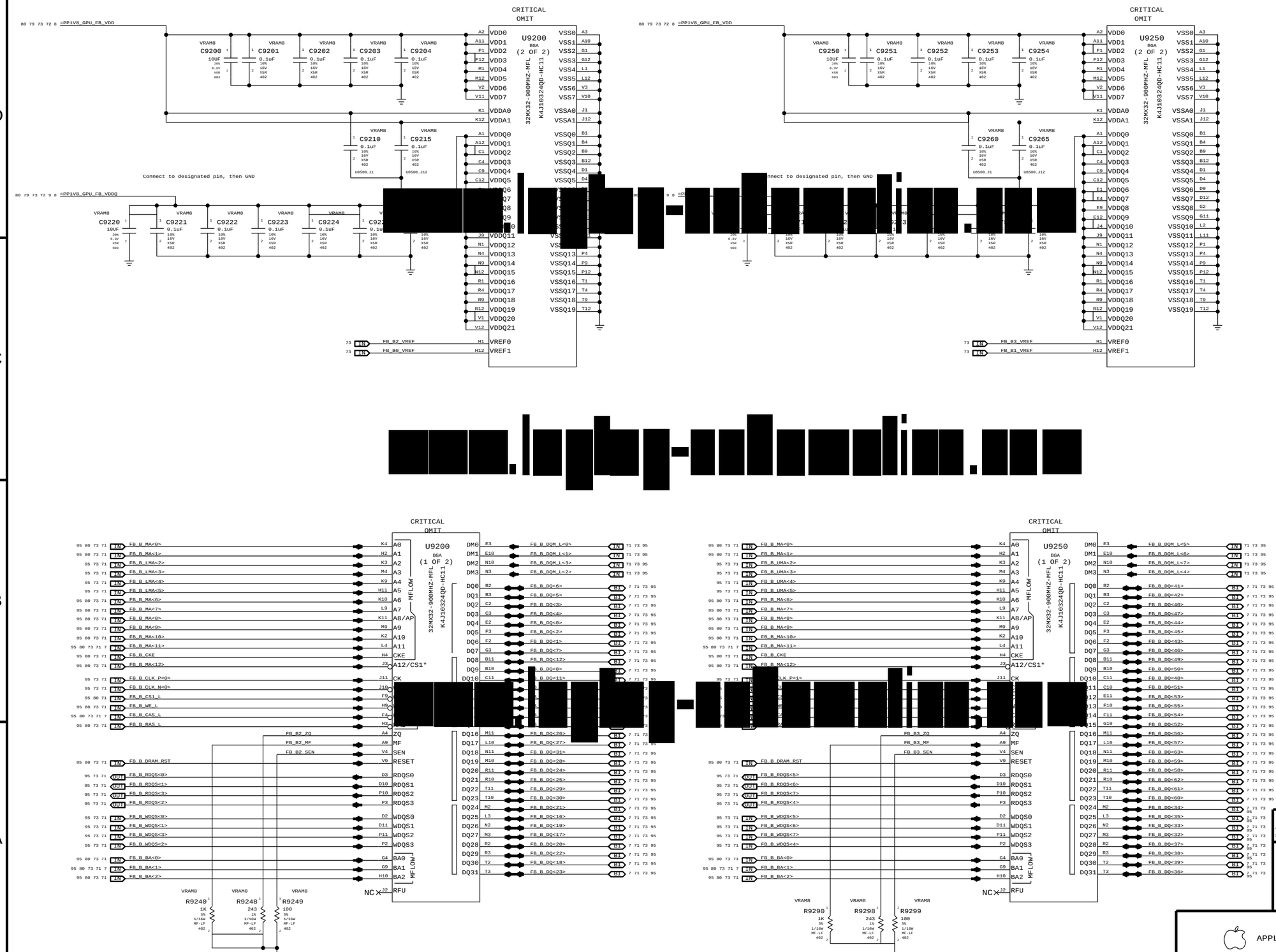
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 79 OF 98	



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM8

GDDR3 Frame Buffer B (Top)

SYNC_MASTER=M88_MLB SYNC_DATE=11/01/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

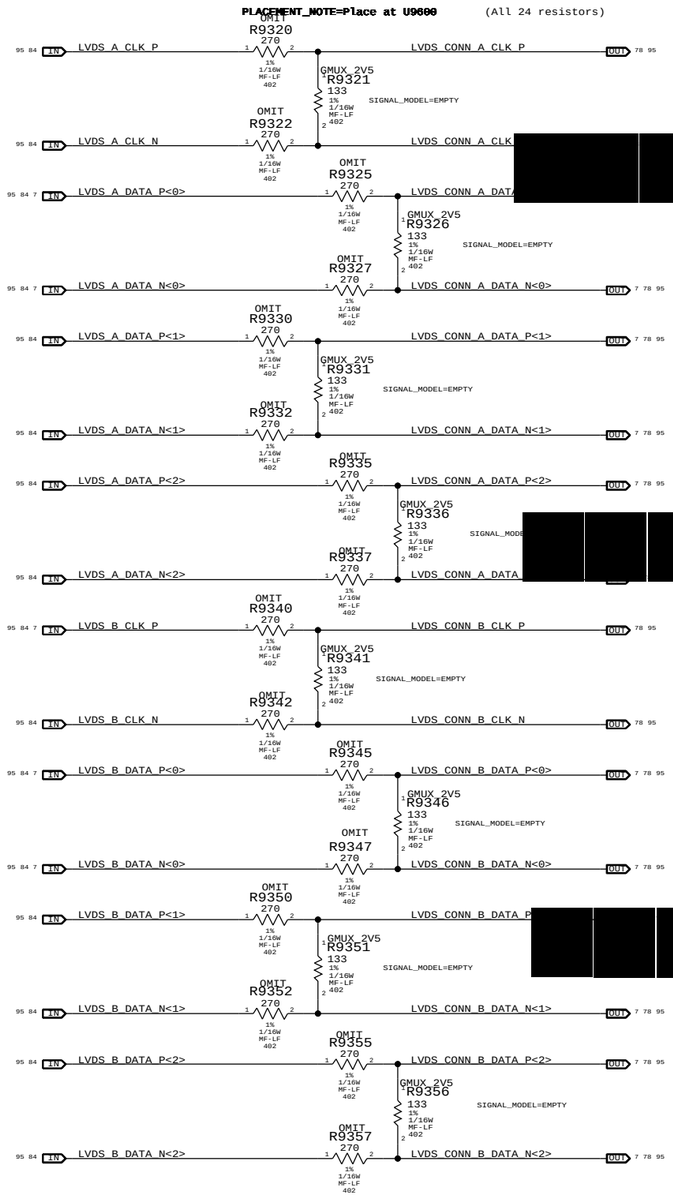
SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 80 OF 98

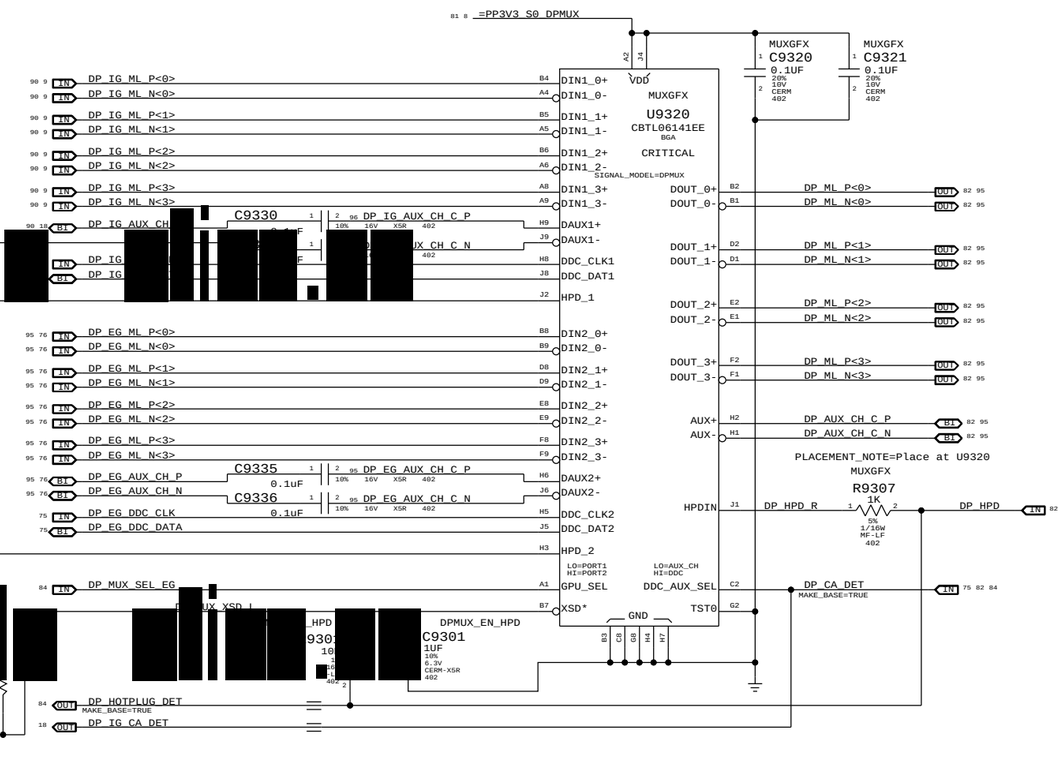
LVDS Transmitter Termination

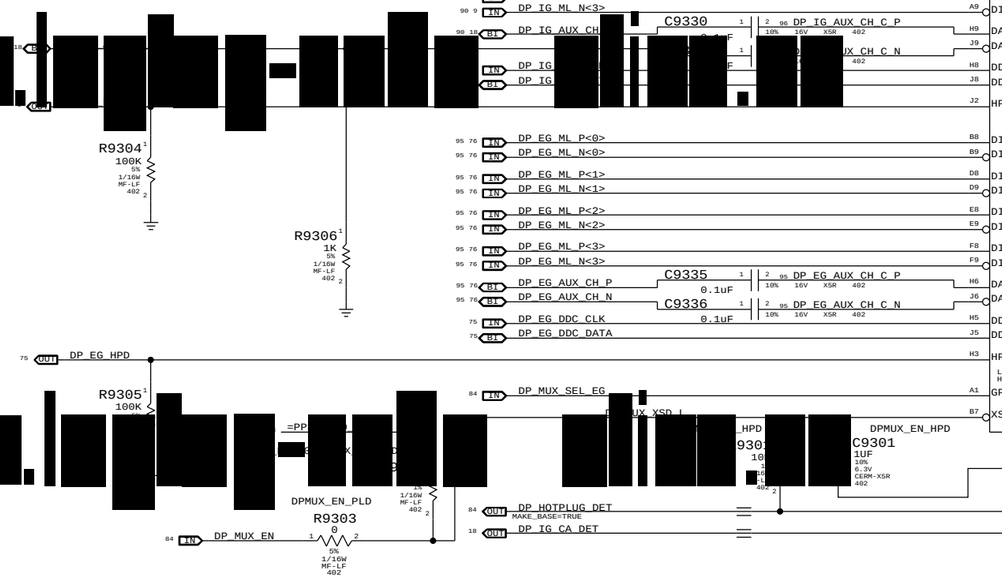
All emulated LVDS outputs require this termination

PLACEMENT_NOTE=Place at U9600 (All 24 resistors)

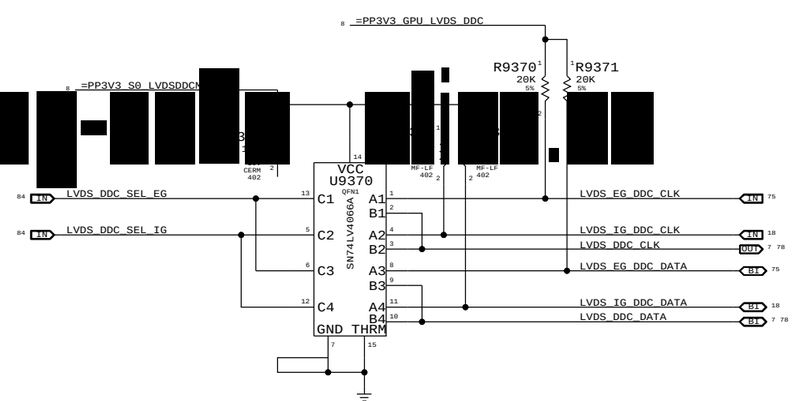


DisplayPort Mux





LVDS DDC MUX



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0517	16	RES,MTL FILM,270 OHM,1%,1/16W,0402,SMD,L	[illegible]		GMUX_2V5
114S0174	16	RES,MTL FILM,1/16W,357 OHM,1,0402,SMD,LF	[illegible]		GMUX_1V8

Muxed Graphics Support

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

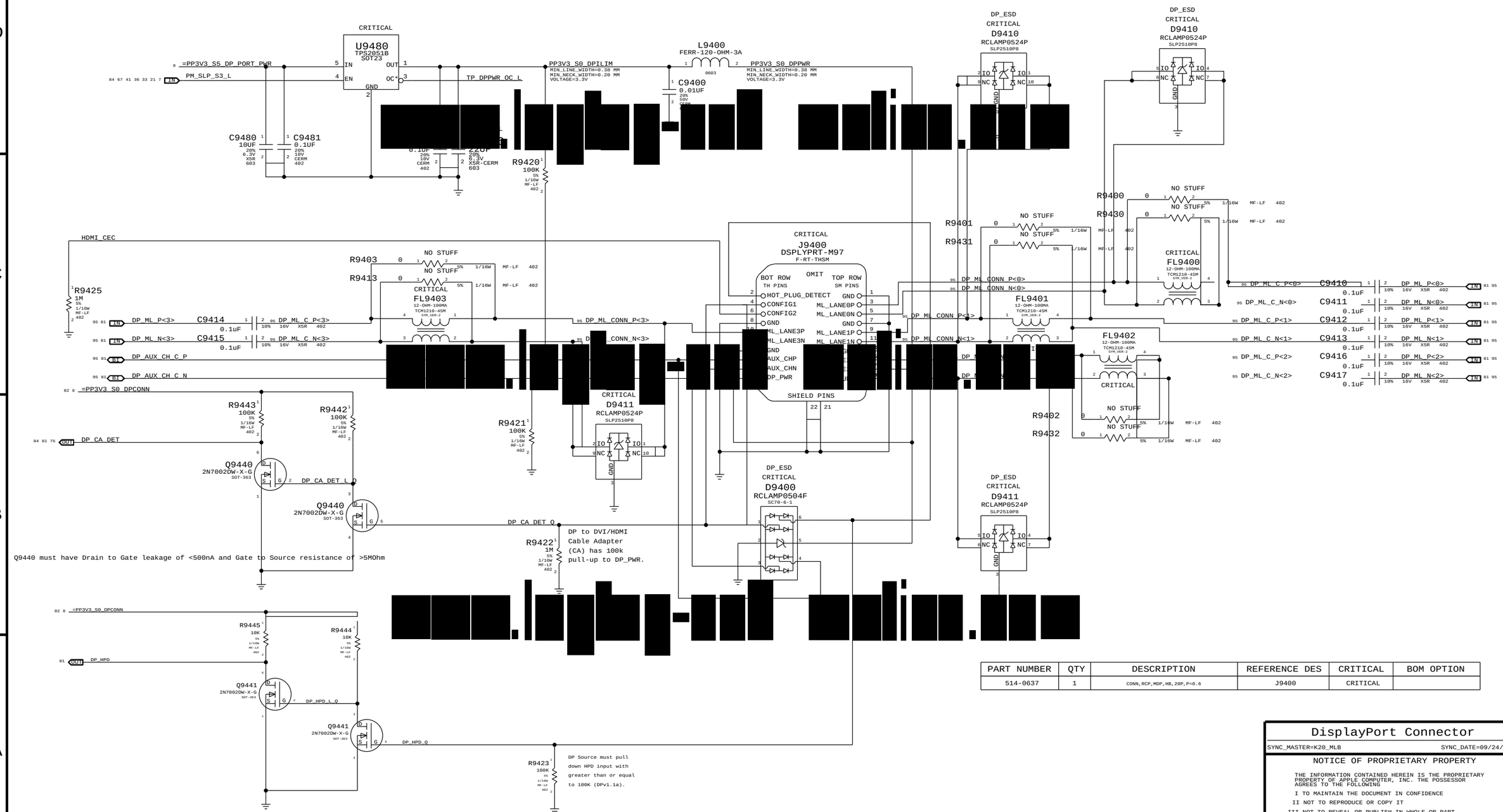
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 81 OF 98	

Port Power Switch



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0637	1	CONN,RCP,MDP,HB,20P,P=0.6	J9400	CRITICAL	

DisplayPort Connector

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

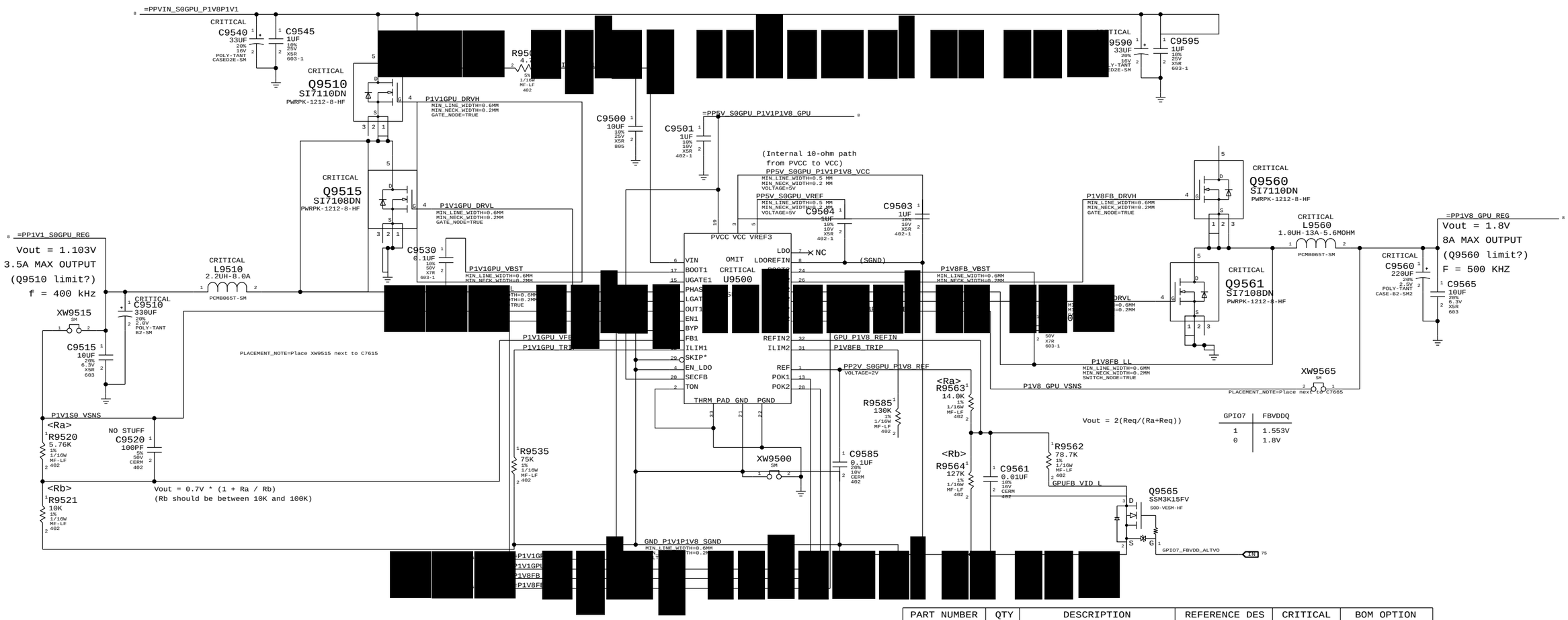
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 82 OF 98	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2312	1	IC,ISL6236,DUAL PWM CNTRL,QFN32	U9500	CRITICAL	

1.1V / 1V8 FB Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

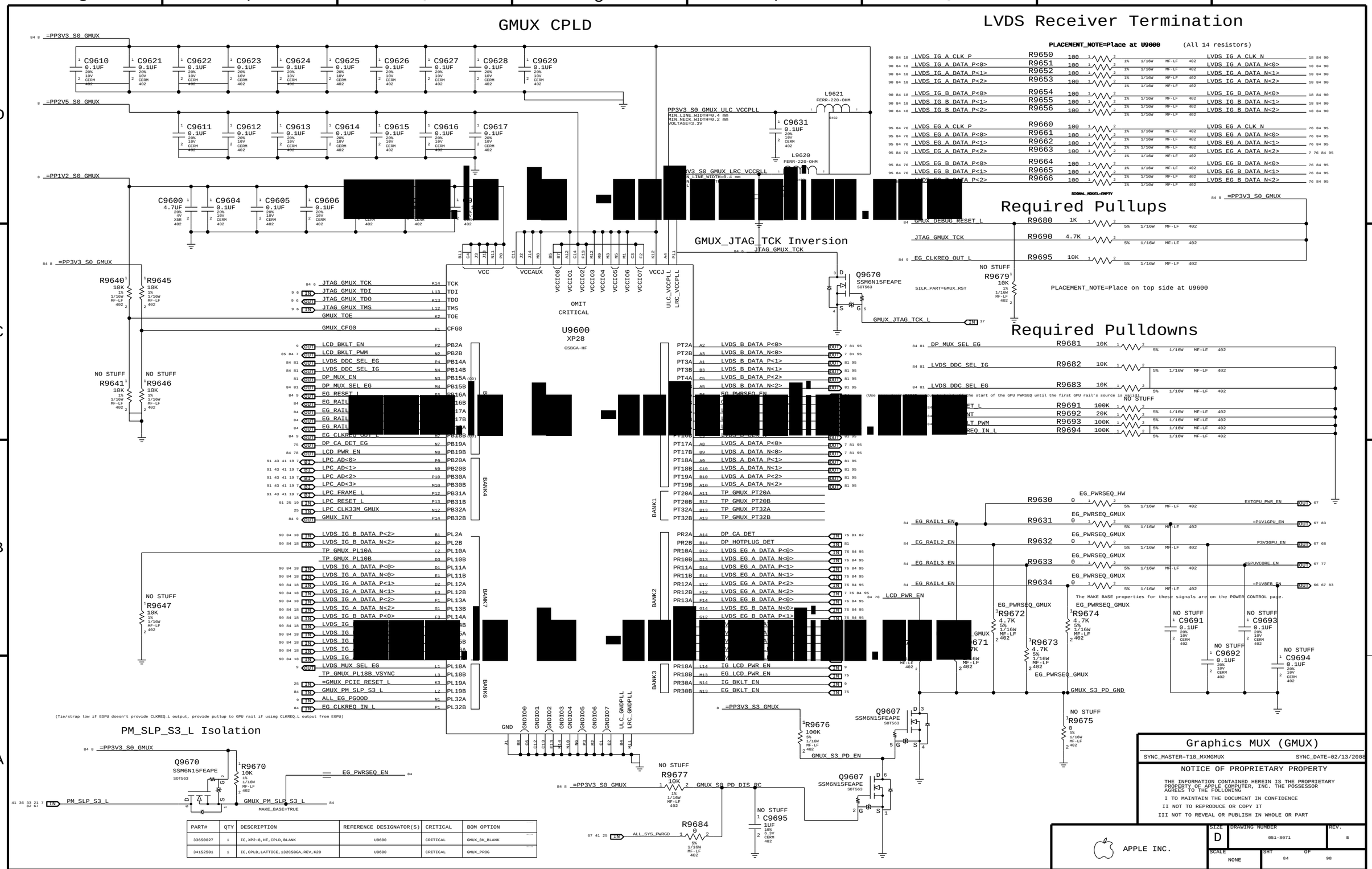
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

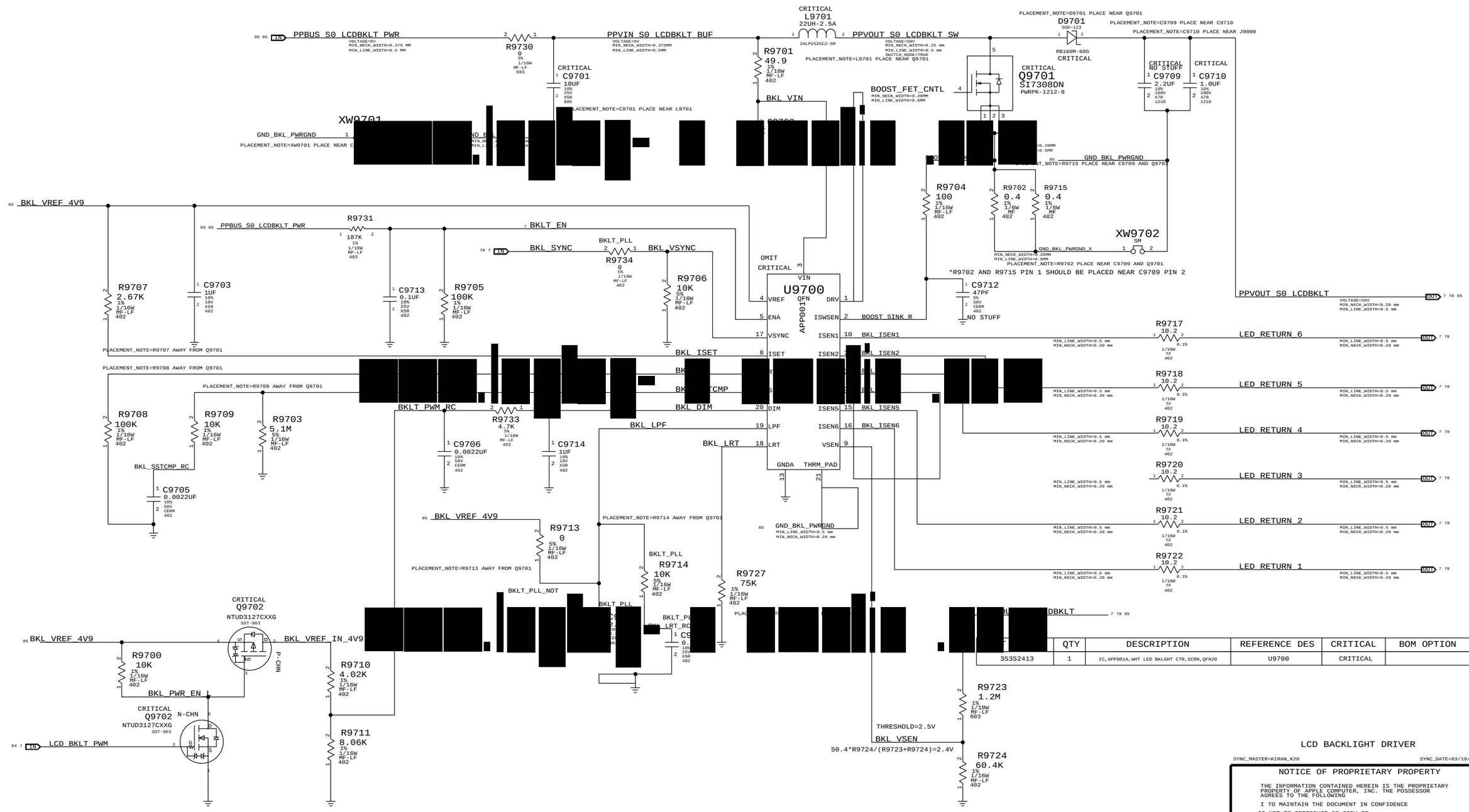
SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 83 OF 98



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
336S0027	1	IC,XP2-8,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_BK_BLANK
341S2501	1	IC,CPLD,LATTICE,132CSBGA,REV,K20	U9600	CRITICAL	GMUX_PROG

*Q9701, D9701, C9709, C9710, L9701, R9702, AND R9715 SHOULD ALL BE PLACED NEAR EACHOTHER.
*BOOST_FET_CNTL AND PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.



QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
1	IC,APP001A,WHT LED BKLGHT CTR,SCRN,QFN20	U9700	CRITICAL	

*R9707, R9708, R9709, R9713, R9714, R9727, AND R9729 SHOULD AWAY FROM BOOST CIRCUIT

LCD BACKLIGHT DRIVER

SYNC_MASTER=KIRAN_K20 SYNC_DATE=03/19/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

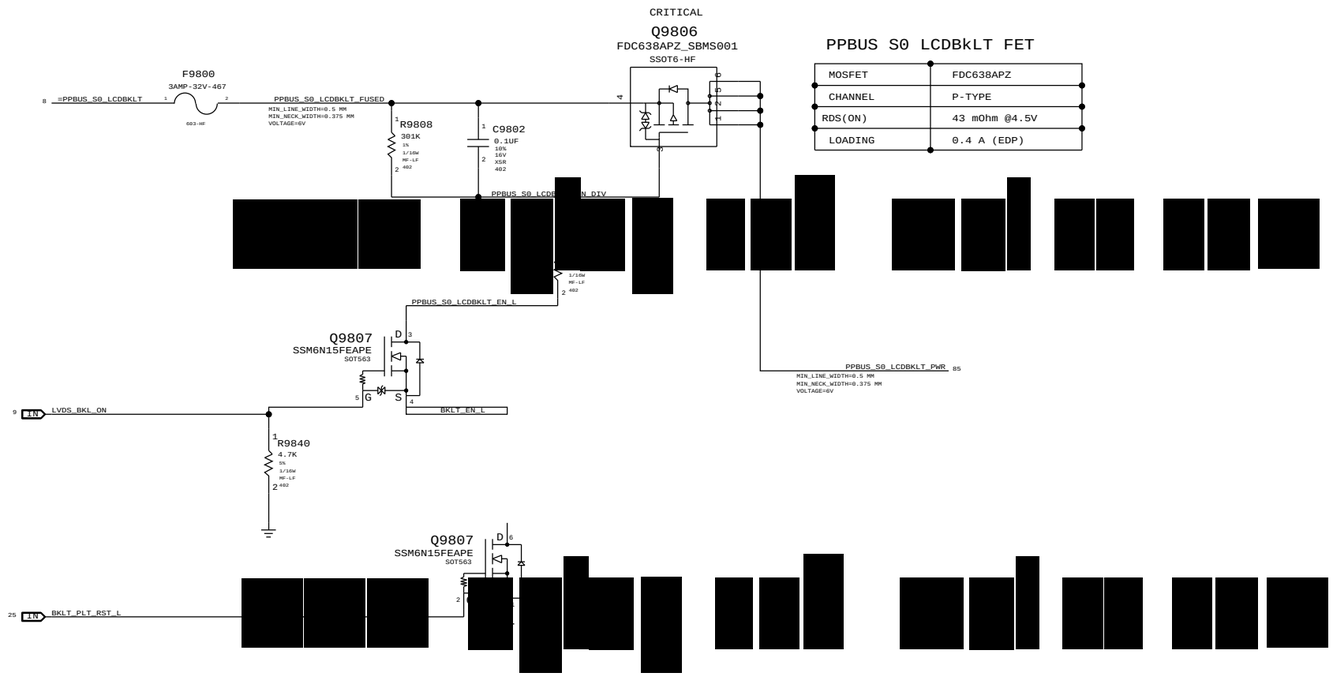
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 85 OF 98	



PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

LCD Backlight Support

SYNC_MASTER=YLEE_K20 SYNC_DATE=07/18/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

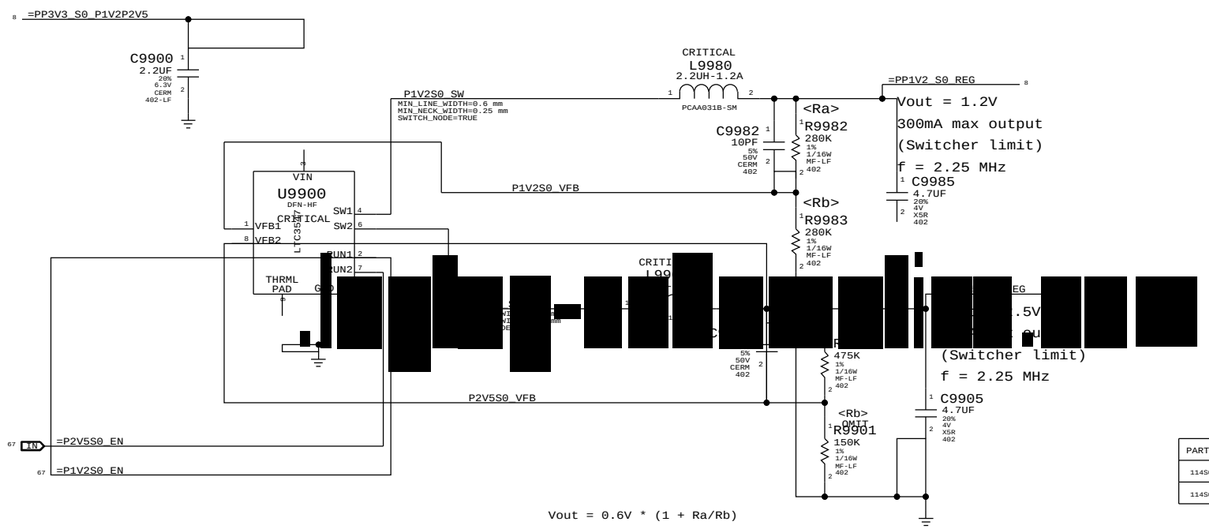
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 86 OF 98

GMUX 1.8V/1.2V S0 Switcher



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0428	1	RES,MTL FILM,1/16W,150K,1,0402,SMD,LF	R9901		GMUX_2V5
114S0447	1	RES,MTL FILM,1/16W,237K,1,0402,SMD,LF	R9901		GMUX_1V8

Misc Power Supplies

SYNC_MASTER=RXU_K20 SYNC_DATE=05/07/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 87 OF 98

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matc[redacted]
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to t[redacted]
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs[redacted]

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matche[redacted]
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	[redacted]	?

SR DG recommends at least 2[redacted]

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_[redacted]	[redacted]	=100_[redacted]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	[redacted]
CLK_FSB	TOP,BOTTOM	[redacted]

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
[redacted]	[redacted]	[redacted]	[redacted]	7 10 14
[redacted]	[redacted]	[redacted]	[redacted]	7 10 14
[redacted]	[redacted]	[redacted]	[redacted]	7 10 14
[redacted]	[redacted]	[redacted]	[redacted]	7 10 14
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	7 10 14
FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9 10 14
FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14
FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	7 10 14
FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	7 10 14
FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	7 10 14
FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	7 10 14
FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	7 10 14
FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9 10 13 14
FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9 10
CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	10 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
[redacted]	[redacted]	[redacted]	[redacted]	10 14
[redacted]	[redacted]	[redacted]	[redacted]	9 10 14
[redacted]	[redacted]	[redacted]	[redacted]	9 10 14
[redacted]	[redacted]	[redacted]	[redacted]	10 14 42 61
[redacted]	[redacted]	[redacted]	[redacted]	10 13 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 14 42
FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10 14
CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10 14
CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9 10 14 61
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10 14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
CPU_IERR_L	CPU_50S		CPU_IERR_L	10
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21 61
(See above)	[redacted]	CPU_AGTL	IMVP_DPRSLPVR	61
[redacted]	[redacted]	[redacted]	[redacted]	10 26
[redacted]	[redacted]	[redacted]	[redacted]	10
[redacted]	[redacted]	[redacted]	[redacted]	10
[redacted]	[redacted]	[redacted]	[redacted]	10
[redacted]	[redacted]	[redacted]	[redacted]	10
XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	6 10 13
XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	6 10
XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	6 10 13
XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	6 10 13
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	6 10 13
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10 13
XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10 13
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	13
	CPU_50S	CPU_8MIL	CPU_VID<6..0>	9 11
	CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	9 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 61
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	61
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	61

FSB 4X Signal Groups

FSB 1X Signals

CPU/FSB Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 88 OF 98	

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

[redacted]

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	[redacted]	[redacted]	[redacted]
MEM_CTRL	[redacted]	[redacted]	[redacted]
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

[redacted]

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	15 27
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 27
[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 27
MEM_A_DQS6	[redacted]	MEM_DQS	MEM_A_DQS_P<6>	15 27
MEM_A_DQS6	[redacted]	MEM_DQS	MEM_A_DQS_N<6>	15 27
[redacted]	[redacted]	[redacted]	[redacted]	15 27
[redacted]	[redacted]	[redacted]	[redacted]	15 27
[redacted]	[redacted]	[redacted]	[redacted]	15 28
[redacted]	[redacted]	[redacted]	[redacted]	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 28
MEM_B_DQ_BYTE3	[redacted]	MEM_DATA	MEM_B_DM<3>	15 28
MEM_B_DQ_BYTE4	[redacted]	MEM_DATA	MEM_B_DM<4>	15 28
[redacted]	[redacted]	[redacted]	[redacted]	15 28
[redacted]	[redacted]	[redacted]	[redacted]	15 28
[redacted]	[redacted]	[redacted]	[redacted]	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 28
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

Memory Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 89 OF 98

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPA[redacted]
CRT	[redacted]

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER [redacted]
DISPLAYPORT	TOP,BOTTO[redacted]
LVDS	TOP,BOTTO[redacted]

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

[redacted]

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	69
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	69
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	9 69
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	9 69
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	9 69
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	9 69
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	69
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	69
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	7 30
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	7 30
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17 30
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17 30
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	7 17 30
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	7 17 30
	PCIE_90D	PCIE	PCIE_FW_R2D_P	35
	PCIE_90D	PCIE	PCIE_FW_R2D_N	35
[redacted]	[redacted]	[redacted]	[redacted]	17 35
[redacted]	[redacted]	[redacted]	[redacted]	17 35
[redacted]	[redacted]	[redacted]	[redacted]	17 35
[redacted]	[redacted]	[redacted]	[redacted]	17 35
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	35
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	35
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P	7 31
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N	7 31
PCIE_EXCARD_R2D	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_P	17 31
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_N	17 31
PCIE_EXCARD_D2R	PCIE_90D	PCIE	PCIE_EXCARD_D2R_P	7 17 31
	PCIE_90D	PCIE	PCIE_EXCARD_D2R_N	7 17 31
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	17 69
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	17 69
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 30
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	17 35
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	17 35
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	17 31
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	17 31
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR	18 24
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y	18 24
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB	18 24
[redacted]	[redacted]	[redacted]	[redacted]	18 24
[redacted]	[redacted]	[redacted]	[redacted]	18 24
[redacted]		[redacted]	[redacted]	18 24
[redacted]		[redacted]	[redacted]	18 24
[redacted]	DP_100D	[redacted]	[redacted]	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0>	9 81
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0>	9 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18 81
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	18 24
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	18 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	18 84
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	18 84
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>	9 18
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	9 18
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	18 84
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	18 84
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	9 18
[redacted]	[redacted]	[redacted]	[redacted]	9 18
[redacted]	[redacted]	[redacted]	[redacted]	18 24
[redacted]	[redacted]	[redacted]	[redacted]	18 24
[redacted]	SATA_100D	[redacted]	[redacted]	20 38
[redacted]	SATA_100D	SATA	SATA_HDD_R2D_C_N	20 38
	SATA_100D	SATA	SATA_HDD_R2D_P	7 38
	SATA_100D	SATA	SATA_HDD_R2D_N	7 38
SATA_HDD_D2R	SATA_100D	SATA	SATA_HDD_D2R_P	20 38
	SATA_100D	SATA	SATA_HDD_D2R_N	20 38
	SATA_100D	SATA	SATA_HDD_D2R_C_P	7 38
	SATA_100D	SATA	SATA_HDD_D2R_C_N	7 38
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	20 38
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20 38
	SATA_100D	SATA	SATA_ODD_R2D_P	7 38
	SATA_100D	SATA	SATA_ODD_R2D_N	7 38
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	20 38
	SATA_100D	SATA	SATA_ODD_D2R_N	20 38
	SATA_100D	SATA	SATA_ODD_D2R_C_P	7 38
	SATA_100D	SATA	SATA_ODD_D2R_C_N	7 38
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	20

MCP Constraints 1

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 90 OF 98

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK			
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	13 19
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	19
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	19
[redacted]				
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	19
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	7 19 41 43 84
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	7 19 41 43 84
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19 25 84
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	19 25
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	25 41
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	7 25 43
USB_EXTA	USB_90D	USB	USB_EXTA_P	20 39
	USB_90D	USB	USB_EXTA_N	20 39
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	9 20
	USB_90D	USB	USB_MINI_N	9 20
USB_EXTD	USB_90D	USB	USB_EXTD_P	9 20
	USB_90D	USB	USB_EXTD_N	9 20
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	20 30
	USB_90D	USB	USB_CAMERA_N	20 30
USB_BT	USB_90D	USB	USB_BT_P	20 30
[redacted]				
USB_EXTB	USB_90D	USB	USB_EXTB_P	20 39
	USB_90D	USB	USB_EXTB_N	20 39
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	20 31
	USB_90D	USB	USB_EXCARD_N	20 31
USB_EXTC	USB_90D	USB	USB_EXTC_P	20 96 98
	USB_90D	USB	USB_EXTC_N	20 96 98
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	7 13 21 44
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	7 13 21 44
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	21 44
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	21 44
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	9 21
	HDA_55S	HDA	HDA_BIT_CLK_R	21
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	21 53
	HDA_55S	HDA	HDA_SYNC_R	21
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	21
	HDA_55S	HDA	HDA_RST_L	21 53
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	21 53
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	21 53
	HDA_55S	HDA	HDA_SDOUT_R	21
[redacted]				
	SPI_55S	SPI	SPI_CLK	52
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	21 43
	SPI_55S	SPI	SPI_MOSI	52
SPI_MISO	SPI_55S	SPI	SPI_MISO	21 43
	SPI_55S	SPI	SPI_MISO_R	52
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	21 43
	SPI_55S	SPI	SPI_CS0_L	

MCP Constraints 2

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 91 OF 98

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

[redacted]

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 33
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	32 33
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18 32
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18 32
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	32
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 32
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	32
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 32
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 32
ENET_RXD	[redacted]	ENET_MII	ENET_RX_CTRL	18 32
[redacted]	[redacted]	[redacted]	[redacted]	18 32
[redacted]	[redacted]	[redacted]	[redacted]	18 32
[redacted]	[redacted]	[redacted]	[redacted]	18 32
[redacted]	[redacted]	[redacted]	[redacted]	18 32
[redacted]	[redacted]	[redacted]	[redacted]	18 32
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	32 34
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	32 34

[redacted]

[redacted]

[redacted]

Ethernet Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 92 OF 98

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING
FW_P0_TPA	FW_110D	FW_TP
FW_P0_TPA	FW_110D	FW_TP
FW_P0_TPB	FW_110D	FW_TP
FW_P0_TPB	FW_110D	FW_TP
FW_P1_TPA	FW_110D	FW_TP
FW_P1_TPA	FW_110D	FW_TP
FW_P1_TPB	FW_110D	FW_TP
FW_P1_TPB	FW_110D	FW_TP

Port 2 Not Used

FW_P0_TPA_P 35 37
FW_P0_TPA_N 35 37
FW_P0_TPB_P 35 37
FW_P0_TPB_N 35 37
FW_P1_TPA_P 35 37
FW_P1_TPA_N 35 37
FW_P1_TPB_P 35 37
FW_P1_TPB_N 35 37

[redacted]

[redacted]

[redacted]

FireWire Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 93 OF 98

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_555	SMB	SMBUS_SMC_A_S3_SCL	7 44
SMBUS_SMC_A_S3_SDA	SMB_555	SMB	SMBUS_SMC_A_S3_SDA	7 44
SMBUS_SMC_B_S0_SCL	SMB_555	SMB	SMBUS_SMC_B_S0_SCL	44
SMBUS_SMC_B_S0_SDA	SMB_555	SMB	SMBUS_SMC_B_S0_SDA	44
SMBUS_SMC_0_S0_SCL	SMB_555	SMB	SMBUS_SMC_0_S0_SCL	44
SMBUS_SMC_0_S0_SDA	SMB_555	SMB	SMBUS_SMC_0_S0_SDA	44
SMBUS_SMC_BSA_SCL	SMB_555	SMB	SMBUS_SMC_BSA_SCL	7 44
SMBUS_SMC_BSA_SDA	SMB_555	SMB	SMBUS_SMC_BSA_SDA	7 44
SMBUS_SMC_MGMT_SCL	SMB_555	SMB	SMBUS_SMC_MGMT_SCL	44
SMBUS_SMC_MGMT_SDA	SMB_555	SMB	SMBUS_SMC_MGMT_SDA	44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	60
[redacted]	[redacted]	[redacted]	[redacted]	60
[redacted]	[redacted]	[redacted]	[redacted]	60
[redacted]	[redacted]	[redacted]	[redacted]	60

[redacted]

[redacted]

[redacted]

SMC Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 94 OF 98

GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	0.095 MM	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

[redacted]

From T18 MXM:

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock le[redacted]
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be wit[redacted]
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals[redacted]
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>	71 72 79
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>	71 72 79
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>	71 72 79
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<12..6>	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CAS_L	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L	71 72 79
FB_AB_CMD_EO	GDDR3_40R55SE	GDDR3_CMD	FB_A_CKE	71 72 79
FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_CS0_L	71 72
FB_AB_CMD_EO	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST	71 72 79
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_LMA<5..2>	71 72 79
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_UMA<5..2>	71 72 79
[redacted]				
	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<0>	71 72 79
	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<1>	71 72 79
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<2>	71 72 79
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<3>	71 72 79
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<7..0>	7 71 72 79
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<15..8>	7 71 72 79
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<23..16>	7 71 72 79
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<31..24>	7 71 72 79
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<0>	71 72 79
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<1>	71 72 79
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<2>	71 72 79
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<3>	71 72 79
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<4>	71 72 79
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<5>	71 72 79
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<6>	71 72 79
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<7>	71 72 79
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<4>	71 72 79
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<5>	71 72 79
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<6>	71 72 79
[redacted]				
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<39..32>	7 71 72 79
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<47..40>	7 71 72 79
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<55..48>	7 71 72 79
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<63..56>	7 71 72 79
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<4>	71 72 79
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<5>	71 72 79
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<6>	71 72 79
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<7>	71 72 79
120 FB_AB_CS1	GDDR3_40R55SE	GDDR3_CMD	FB_A_CS1_L	71 79

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>	71 73 80
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>	71 73 80
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>	71 73 80
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>	71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>	71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<12..6>	7 71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>	7 71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L	71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CAS_L	7 71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L	71 73 80
FB_CD_CMD_EO	GDDR3_40R55SE	GDDR3_CMD	FB_B_CKE	71 73 80
FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_CS0_L	7 71 73
FB_CD_CMD_EO	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST	71 73 80
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_LMA<5..2>	71 73 80
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_UMA<5..2>	71 73 80
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<0>	71 73 80
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<1>	71 73 80
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<2>	71 73 80
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<3>	71 73 80
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<0>	71 73 80
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<1>	71 73 80
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<2>	71 73 80
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<3>	71 73 80
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<7..0>	7 71 73 80
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<15..8>	7 71 73 80
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<23..16>	7 71 73 80
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<31..24>	7 71 73 80
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<0>	71 73 80
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<1>	71 73 80
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<2>	71 73 80
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<3>	71 73 80
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<4>	71 73 80
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<5>	71 73 80
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<6>	71 73 80
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<7>	71 73 80
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<4>	71 73 80
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<5>	71 73 80
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<6>	71 73 80
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<7>	71 73 80
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<39..32>	7 71 73 80
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<47..40>	7 71 73 80
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<55..48>	7 71 73 80
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<63..56>	7 71 73 80
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<4>	71 73 80
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<5>	71 73 80
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<6>	71 73 80
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<7>	71 73 80
120 FB_CD_CS1	GDDR3_40R55SE	GDDR3_CMD	FB_B_CS1_L	71 80

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
142 LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	81 84
142 LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	81 84
139 LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	7 81 84
139 LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	7 81 84
152 LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	7 81 84
152 LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	81 84
202 LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	
202 LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	
187	LVDS_100D	LVDS	LVDS_CONN_A	
187	LVDS_100D	LVDS	LVDS_CONN_A	
154	LVDS_100D	LVDS	LVDS_CONN_B	
195	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_N	7 78
195	LVDS_100D	LVDS	LVDS_CONN_A_CLK_P	78 81
193	LVDS_100D	LVDS	LVDS_CONN_A_CLK_N	78 81
193	LVDS_100D	LVDS	LVDS_CONN_A_DATA_P<2..0>	7 78 81
192	LVDS_100D	LVDS	LVDS_CONN_A_DATA_N<2..0>	7 78 81
196	LVDS_100D	LVDS	LVDS_CONN_B_CLK_P	78 81
196	LVDS_100D	LVDS	LVDS_CONN_B_CLK_N	78 81
197	LVDS_100D	LVDS	LVDS_CONN_B_DATA_P<2..0>	7 78 81
197	LVDS_100D	LVDS	LVDS_CONN_B_DATA_N<2..0>	7 78 81
182 DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	82
182	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	82
152 DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	81 82
152	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	81 82
202 DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	82
202	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	82
150 DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	81 82
150 DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	81 82

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
(CK505_DOT96)	CLK_SLOW_555	CLK_SLOW	GPU_CLK27M	75
CK505_CLK27MSS	CLK_SLOW_555	CLK_SLOW	GPU_CLK27M_SS	75
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_P	76 84
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_N	76 84
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_P<2..0>	76 84
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_N<2..0>	7 76 84
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_P<2..0>	76 84
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_N<2..0>	76 84
[redacted]				
		DISPLAYPORT		
		DISPLAYPORT		
		DISPLAYPORT		
		DISPLAYPORT		
		DISPLAYPORT		
150	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_N	81

GPU (G96) Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 95 OF 98	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	FSB_DSTB	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	[redacted]		

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERR[redacted]	[redacted]	[redacted]
MEM_40S_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERR[redacted]	[redacted]	[redacted]
MEM_70D OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERR[redacted]	[redacted]	[redacted]
MEM_70D_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane)but not next to VDD island.
Forces power-referenced memory signals (CLK,ADDR,CTRL) to not route on ISL3, ISL4 & ISL10(GND-referenced planes).

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
DP_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

FLASH MEMORY BUS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FLSH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_MDI_100D	ENETCONN	ENETCONN_P<3..0>	34
	ENET_MDI_100D	ENETCONN	ENETCONN_N<3..0>	34
1146	SATA_100D	SATA	SATA_ODD_R2D_UF_P	38
1145	SATA_100D	SATA	SATA_ODD_R2D_UF_N	38
1144	SATA_100D	SATA	SATA_ODD_D2R_UF_P	38
1142	SATA_100D	SATA	SATA_ODD_D2R_UF_N	38
1143	SATA_100D	SATA	SATA_HDD_D2R_UF_P	38
1140	SATA_100D	SATA	SATA_HDD_D2R_UF_N	38
1141	SATA_100D	SATA	SATA_HDD_R2D_UF_P	38
1139	SATA_100D	SATA	SATA_HDD_R2D_UF_N	38
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	MCPCOREISNS_P	46 64
	SENSE_1TO1_55S	SENSE	MCPCOREISNS_N	46 64
1312 CPUTHMSNS_D2_DP	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	47
1311	THERM_1TO1_55S	THERM	CPUTHMSNS[redacted]	47
[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	47 75
1138 DP	THERM_1TO1_55S	THERM	MCPTHMSNS_D_P	7 47
1137	THERM_1TO1_55S	THERM	MCPTHMSNS_D_N	7 47
1135 MCP_THERMD_DP	THERM_1TO1_55S	THERM	MCP_THMDIODE_P	21 47
1136	THERM_1TO1_55S	THERM	MCP_THMDIODE_N	21 47
1158 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	1V05CPUISNS_R_P	46
1157	SENSE_1TO1_55S	SENSE	1V05CPUISNS_R_N	46
1155 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_R_P	46
1154	SENSE_1TO1_55S	SENSE	DDRISNS_R_N	46
1153 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_P	46
1152	SENSE_1TO1_55S	SENSE	GPUISENS_N	46
1151 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	1V05CPU_P	46 65
1150	SENSE_1TO1_55S	SENSE	1V05CPU_N	46 65
1149 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_P	46
1148	SENSE_1TO1_55S	SENSE	DDRISNS_N	46
1150 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPU_P	46
1147	SENSE_1TO1_55S	SENSE	P1V8GPU_N	46
1186 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_P	45
1185	SENSE_1TO1_55S	SENSE	ISNS_CPU_N	45
		GND	GND	
[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
1187	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_N	
1188 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_P	46
1189	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_N	46
1240 ASIC_CNTRLMEM1	FLSH_55S		NF_CLE_R	96
1240 ASIC_CNTRLMEM1	FLSH_55S		NF_ALE_R	96
1240 ASIC_CNTRLMEM1	FLSH_55S		NF_CE0_L_R	96
1240 ASIC_CNTRLMEM1	FLSH_55S		NF_CE1_L_R	96
1242 ASIC_CNTRLMEM1	FLSH_55S		NF_RE0_L_R	96
1243 ASIC_CNTRLMEM1	FLSH_55S		NF_WE0_L_R	96
1230 ASIC_CNTRLMEM2	FLSH_55S		NF_CLE_R	96
1240 ASIC_CNTRLMEM2	FLSH_55S		NF_ALE_R	96
1230 ASIC_CNTRLMEM2	FLSH_55S		NF_CE0_L_R	96
1230 ASIC_CNTRLMEM2	FLSH_55S		NF_CE1_L_R	96
1230 ASIC_CNTRLMEM2	FLSH_55S		NF_RE0_L_R	96
1230 ASIC_CNTRLMEM2	FLSH_55S		NF_WE0_L_R	96
1233 ASIC_CNTRLMEM3	FLSH_55S		NF_CLE	96
[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
1222 ASIC_CNTRLMEM2	FLSH_55S		NF_CLE	96
1227 ASIC_CNTRLMEM2	FLSH_55S		NF_ALE	96
1220 ASIC_CNTRLMEM2	FLSH_55S		NF_CE0_L	96
1221 ASIC_CNTRLMEM2	FLSH_55S		NF_CE1_L	96
1222 ASIC_CNTRLMEM2	FLSH_55S		NF_RE0_L	96
1223 ASIC_CNTRLMEM2	FLSH_55S		NF_WE0_L	96

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1160	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	7 30
1159	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	7 30
1160	1TO1_DIFFPAIR		CHGR_CSI_R_P	60
1159	1TO1_DIFFPAIR		CHGR_CSI_R_N	60
1157	1TO1_DIFFPAIR		CHGR_CSO_R_P	45 60
1156	1TO1_DIFFPAIR		CHGR_CSO_R_N	45 60
1177 (USB_EXTA)	USB_900	USB	USB2_EXTA_MUXED_P	39
1174 (USB_EXTA)	USB_900	USB	USB2_EXTA_MUXED_N	39
1172 (USB_EXTA)	USB_900	USB	USB2_LT1_P	7 39
1169 (USB_EXTA)	USB_900	USB	USB2_LT1_N	7 39
1171 (USB_EXTD)	USB_900	USB	CONN_TPAD_USB_P	
1170 (USB_EXTD)	USB_900	USB	CONN_TPAD_USB_N	
1168 (USB_CAMERA)	USB_900	USB	USB_CAMERA_CONN_P	7 30
1167 (USB_CAMERA)	USB_900	USB	USB_CAMERA_CONN_N	7 30
[redacted]	USB_900	USB	CONN_USB2_BT_P	7 30
[redacted]	USB_900	USB	CONN_USB2_BT_N	7 30
[redacted]	USB_900	USB	USB_LT2_P	7 39
[redacted]	USB_900	USB	USB_LT2_N	7 39
[redacted]	USB_900	USB	USB2_EXCARD_CONN_P	7 31
[redacted]	USB_900	USB	USB2_EXCARD_CONN_N	7 31
1193	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_P	81
1194	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_N	81
1197 MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	
1198	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	
1199 PCIE_FC_R2D	PCIE_90D	PCIE	PCIE_FC_R2D_C_P	
1200	PCIE_90D	PCIE	PCIE_FC_R2D_C_N	
1192 PCIE_FC_D2R	PCIE_90D	PCIE	PCIE_FC_D2R_P	
1187	PCIE_90D	PCIE	PCIE_FC_D2R_N	
1193	PCIE_90D	PCIE	PCIE_FC_R2D_P	
1194	PCIE_90D	PCIE	PCIE_FC_R2D_N	
1195	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_N	7 31
1196	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_P	7 31
1198 SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L1_OUT_P	7 56 57
1197	DIFFPAIR	AUDIO	SPKRAMP_L1_OUT_N	7 56 57
1201 SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L2_OUT_P	7 56 57
1200	DIFFPAIR	AUDIO	SPKRAMP_L2_OUT_N	7 56 57
1199 SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R1_OUT_P	7 56 57
1202	DIFFPAIR	AUDIO	SPKRAMP_R1_OUT_N	7 56 57
1192 SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R2_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_R2_OUT_N	7 56 57
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_LFE_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_LFE_OUT_N	7 56 57
1210	USB_900	USB	USB_EXTC_P	20 91 98
1209	USB_900	USB	USB_EXTC_N	20 91 98
1212	USB_900	USB	USB_LT3_P	7 98
1211	USB_900	USB	USB_LT3_N	7 98

Project Specific Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 96 OF 98	

M99 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STA[redacted]		

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	[redacted]	?
2:1_SPACIN[redacted]	[redacted]	[redacted]	[redacted]
2.5:1_SPACIN[redacted]	[redacted]	[redacted]	[redacted]
3:1_SPACIN[redacted]	[redacted]	[redacted]	[redacted]
4:1_SPACIN[redacted]	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NOTE:From T18 MLB, changed to reflect M99 stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
[redacted]_DIELE[redacted]TR[redacted]	[redacted]	0.140 MM[redacted]	?
[redacted]_DIELE[redacted]TR[redacted]	[redacted]	0.210 MM[redacted]	?
[redacted]_DIELE[redacted]TR[redacted]	[redacted]	0.280 MM[redacted]	?
5X_DIELECTRIC	*	0.350 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.135 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	[redacted]	[redacted]
70_OHM_DIFF	ISL3,ISL4	Y	0.160 MM	0.160 MM			
70_OHM_DIFF	ISL9,ISL10	Y	0.160 MM	0.160 MM			
70_OHM_DIFF	ISL2,ISL11	Y	0.170 MM	0.170 MM			
70_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.095 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	0.1[redacted]	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.095 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK	DIFF[redacted]
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDAR[redacted]	[redacted]
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		[redacted]
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.095 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

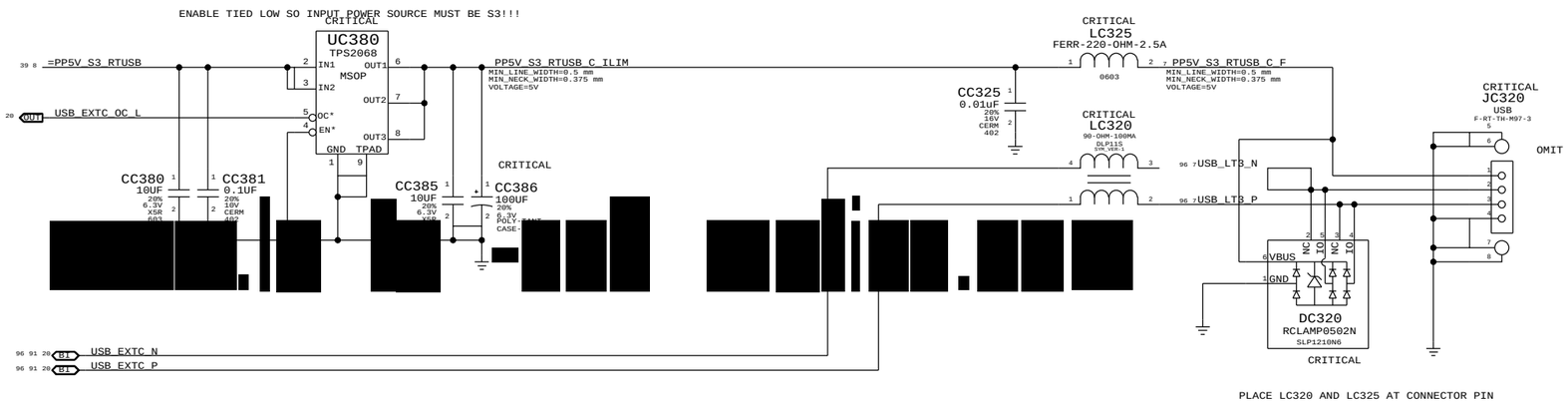
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 97 OF 98

Port Power Switch

LEFT USB PORT C



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
[redacted]514-0638	1	CONN,RCPT,USB,HB,4P	JC320	CRITICAL	

[redacted]

[redacted]

PROJECT SPECIFIC CONNS

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE NONE SHT 98 OF 98